

Eight-Channel Isolated Analog Input Module for Signal Conditioning

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About This Manual

This manual describes the electrical and mechanical aspects of the SCXI-1120 and contains information concerning its operation and programming. The SCXI-1120 is a class I module that operates as eight isolated input channels. Refer to your chassis manual for a description of the different module classes. Each channel is isolated and independently configurable via jumpers. Refer to your chassis manual for a description of the different module classes. The SCXI-1120 is a member of the National Instruments Signal Conditioning eXtensions for Instrumentation (SCXI) Series for the National Instruments data acquisition plug-in boards. This board is designed for low-cost signal conditioning of thermocouples, volt sources, millivolt sources, and 4 to 20 mA sources or 0 to 20 mA process-current sources where high common-mode voltages exist.

This manual describes the installation, theory of operation, and basic programming considerations for the SCXI-1120.

Organization of This Manual

The SCXI-1120 User Manual is organized as follows:

- Chapter 1, *Introduction*, describes the SCXI-1120; lists the contents of your SCXI-1120 kit; describes the optional software, optional equipment, and custom cables; and explains how to unpack the SCXI-1120 kit.
- Chapter 2, *Configuration and Installation*, describes the SCXI-1120 jumper configurations, installation of the SCXI-1120 into the SCXI chassis, signal connections to the SCXI-1120, and cable wiring.
- Chapter 3, *Theory of Operation*, contains a functional overview of the SCXI-1120 module and explains the operation of each functional unit making up the SCXI-1120.
- Chapter 4, *Register Descriptions*, describes in detail the SCXI-1120 Module ID Register, the Configuration Register, the Slot 0 registers, and multiplexer addressing.
- Chapter 5, *Programming*, contains a functional programming description of the SCXI-1120 and Slot 0.
- Appendix A, Specifications, lists the specifications for the SCXI-1120.
- Appendix B, *Rear Signal Connector*, describes the pinout and signal names for the SCXI-1120 50-pin rear signal connector, including a description of each connection.
- Appendix C, *SCXIbus Connector*, describes the pinout and signal names for the SCXI-1120 96-pin SCXIbus connector, including a description of each connection.

- Appendix D, *SCXI-1120 Front Connector*, describes the pinout and signal names for the SCXI-1120 front connector, including a description of each connection.
- Appendix E, *SCXI-1120 Cabling*, describes how to use and install the hardware accessories for the SCXI-1120.
- Appendix F, *Revision A and B Photo and Parts Locator Diagrams*, contains a photograph of the Revision A and B SCXI-1120 signal conditioning module and the general and detailed parts locator diagrams.
- Appendix G, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products and manuals.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms.
- The *Index* contains an alphabetical list of key terms and topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual.

italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
Lab board	Lab board refers to the Lab-LC, Lab-NB, Lab-PC, and Lab-PC+ boards, unless otherwise noted.
MC	MC refers to the Micro Channel series computers.
MIO board	MIO board refers to the AT-MIO-16, AT-MIO-16D, AT-MIO-16F-5, AT-MIO-16X, AT-MIO-64F-5, MC-MIO-16, NB-MIO-16, and NB-MIO-16X series of multichannel I/O data acquisition boards.
monospace	Lowercase text in this font denotes text or characters that are to be literally input from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, variables, filenames, and extensions, and for statements and comments taken from program code.
NB	NB refers to the NuBus series computers.
PC	PC refers to the IBM PC/XT, the IBM PC AT, and compatible computers.
SCXIbus	SCXIbus refers to the backplane in the chassis. A signal on the backplane is referred to as the SCXIbus <signal name=""> line (or signal). The</signal>

SCXIbus descriptor may be omitted when the meaning is clear. Descriptions of all SCXIbus signals are given in Appendix C, *SCXIbus Connector*.

Slot 0 Slot 0 refers to the power supply and control circuitry in the SCXI chassis.

Abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms are listed in the *Glossary*.

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- Your DAQ board user manual
- Your SCXI chassis user manual

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix G, *Customer Communication*, at the end of this manual.

Chapter 1 Introduction

This chapter describes the SCXI-1120; lists the contents of your SCXI-1120 kit; describes the optional software, optional equipment, and custom cables; and explains how to unpack the SCXI-1120 kit.

The SCXI-1120 is a class I module consisting of eight isolated input channels. The SCXI-1120 is a module for signal conditioning of thermocouples, volt sources, millivolt sources, 4 to 20 mA current sources, and 0 to 20 mA process-current sources. Refer to your chassis manual for a description of the different module classes. If external excitation is provided, thermistors, RTDs, and strain gauges can also be measured. The SCXI-1120 can operate in two output modes—in the Parallel-Output mode with all eight input channels connected in parallel to eight data acquisition board channels, or in the Multiplexed-Output mode with all eight channels multiplexed into a single data acquisition board channel.

The SCXI-1120 operates with full functionality with the National Instruments MIO-16 boards. You can use the Lab-NB, the Lab-PC, the Lab-PC+, the Lab-LC, and the PC-LPM-16 boards with the SCXI-1120, but these boards cannot scan the module when it is configured in the Multiplexed-Output mode. These boards can perform only single-channel reads in this mode. You can also use the SCXI-1120 with other systems that comply with the specifications given in Chapter 2, *Configuration and Installation*. You can multiplex several SCXI-1120s into a single channel, thus greatly increasing the number of analog input signals that can be digitized.

The addition of a shielded terminal block provides screw terminals for easy signal attachment to the SCXI-1120. In addition, a temperature sensor for cold-junction compensation of thermocouples is included on the terminal block. This cold-junction reference (CJR) is either multiplexed along with the eight channels or connected by jumpers to a different channel of the data acquisition board.

With the SCXI-1120, the SCXI chassis can serve as a fast-scanning signal conditioner for laboratory testing, production testing, and industrial process monitoring.

What Your Kit Should Contain

The contents of the SCXI-1120 kit (part number 776572-20) are listed as follows.

Kit Component	Part Number
SCXI-1120 module	181695-01
SCXI-1120 User Manual	320425-01

If your kit is missing any of the components, contact National Instruments.

Optional Software

This manual contains complete instructions for directly programming the SCXI-1120. You can order separate software packages for controlling the SCXI-1120 from National Instruments.

When you combine the PC, AT, and MC data acquisition boards with the SCXI-1120, you can use LabVIEW for Windows or LabWindows for DOS. LabVIEW and LabWindows are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows enhances Microsoft C and QuickBASIC. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

Your National Instruments data acquisition board is shipped with the NI-DAQ software. NI-DAQ has a library of functions that can be called from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer, SCXI, RTSI, and self-calibration. NI-DAQ maintains a consistent software interface among its different versions so you can switch between platforms with minimal modifications to your code.

You can also use the SCXI-1120, together with the PC, AT, and MC data acquisition boards, with NI-DAQ software for DOS/Windows/LabWindows. NI-DAQ software for DOS/Windows/LabWindows comes with language interfaces for Professional BASIC, Turbo Pascal, Turbo C, Turbo C++, Borland C++, and Microsoft C for DOS; and Visual Basic, Turbo Pascal, Microsoft C with SDK, and Borland C++ for Windows. NI-DAQ software for DOS/Windows/LabWindows is on high-density 5.25 in. and 3.5 in. diskettes.

You can use the SCXI-1120, together with the NB Series data acquisition boards, with LabVIEW, a software system that features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments boards, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software for Macintosh.

You can also use the SCXI-1120, combined with the NB Series data acquisition boards, with NI-DAQ software for Macintosh. NI-DAQ software for Macintosh, which is shipped with all National Instruments Macintosh data acquisition boards, comes with language interfaces for MPW C, THINK C, Pascal, and Microsoft QuickBASIC. Any language that uses Device Manager Toolbox calls can access NI-DAQ software for Macintosh.

Optional Equipment

Eq	uipment	Part Number
SCXI-1320 front termin	al block	776573-20
SCXI-1328 high-accura	cy isothermal terminal block	776573-28
SCXI-1330 32-pin conn	ector-and-shell assembly	776573-30
SCXI-1340 cable assem	bly	776574-40
SCXI-1341 Lab-NB/Lab	p-PC/Lab-PC+ cable assembly	776574-41
SCXI-1342 PC-LPM-16	cable assembly	776574-42
SCXI-1343 rear screw to	erminal adapter	776574-43
SCXI-1344 Lab-LC cab	le assembly	776574-44
SCXI-1346 shielded mu	ltichassis cable adapter	776574-46
SCXI-1347 SCXI shield	ed cable assembly	
	with 1 m cable	776574-471
	with 2 m cable	776574-472
	with 5 m cable	776574-475
	with 10 m cable	776574-470
SCXI-1349 SCXI shield	ed cable assembly	
	with 1 m cable	776574-491
	with 2 m cable	776574-492
	with 5 m cable	776574-495
	with 10 m cable	776574-490
SCXI-1350 multichassis	adapter	776575-50
SCXI process-current resistor kit		776582-01
Standard ribbon cable	0.5 m	180524-05
	1.0 m	180524-10
NB6 cable		
	0.5 m	181305-01
	1.0 m	181305-10

Refer to the *Signal Connections* section in Chapter 2, *Configuration and Installation*, and to Appendix E, *SCXI-1120 Cabling*, for additional information on cabling, connectors, and adapters.

Custom Cables

The SCXI-1120 rear signal connector is a 50-pin male ribbon-cable header. The manufacturer part number used by National Instruments for this header is as follows:

• AMP Inc. (part number 1-103310-0)

The mating connector for the SCXI-1120 rear signal connector is a 50-position polarized ribbon-socket connector with strain relief. National Instruments uses a polarized or keyed connector to prevent inadvertent upside-down connection to the SCXI-1120. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

Standard 50-conductor, 28 AWG, stranded ribbon cables that can be used with these connectors are as follows:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

The SCXI-1120 front connector is a 32-pin DIN C male connector with columns A and C even pins only. The manufacturer part number used by National Instruments for this connector is as follows:

• Panduit Corporation (part number 100-932-023)

The mating connector for the SCXI-1120 front connector is a 32-pin DIN C female connector. National Instruments uses a polarized connector to prevent inadvertent upside-down connection to the SCXI-1120. Recommended manufacturer part numbers for this mating connector are as follows:

- Panduit Corporation (part number 100-932-434; straight-solder eyelet pins)
- Panduit Corporation (part number 100-932-633; right-angle pins)

These connectors were selected to meet UL 1950 and UL 1244 for 1,500 Vrms isolation.

Unpacking

Your SCXI-1120 module is shipped in an antistatic package to prevent electrostatic damage to the module. Several components on the module can be damaged by electrostatic discharge. To avoid such damage in handling the module, take the following precautions:

- Touch the antistatic package to a metal part of your SCXI chassis before removing the module from the package.
- Remove the module from the package and inspect the module for loose components or any other sign of damage. Notify National Instruments if the module appears damaged in any way. *Do not* install a damaged module into your SCXI chassis.

Chapter 2 Configuration and Installation

This chapter describes the SCXI-1120 jumper configurations, installation of the SCXI-1120 into the SCXI chassis, signal connections to the SCXI-1120, and cable wiring.

Module Configuration

The SCXI-1120 includes 46 jumpers that are shown in the parts locator diagrams in Figures 2-1 and 2-2.

Figure 2-1. SCXI-1120 General Parts Locator Diagram

Figure 2-2 shows a detailed parts locator diagram of the SCXI-1120.

Figure 2-2. Detailed Parts Locator Diagram

The jumpers are used as follows:

- Fixed jumpers
 - On Revision A and B modules, jumper W42 is unused and should not be connected.
 - Jumper W45 is reserved and should not be reconfigured.
 - On Revision A and B modules, jumper W44 carries the SLOT0SEL* signal from the rear signal connector, after buffering, to the SCXIbus INTR* line and should be left in the factory-default position (position 1). On Revision C and later modules, jumper W44 does not exist.
- User-configurable jumpers
 - Jumper W43 carries the SCXIbus MISO line, after buffering, to the SERDATOUT signal on the rear signal connector.
 - On Revision C and later modules, jumper 42 connects a pullup resistor to the SERDATOUT signal on the rear signal connector.
 - Jumper W46 configures the guard, the analog output ground, and enables the Pseudodifferential Reference mode.
 - Jumpers W1 through W8 configure the first-stage gain of channels 0 through 7, respectively.
 - Jumpers W9 through W16 configure the second-stage gain of channels 0 through 7, respectively.
 - Jumpers W17 through W24 configure the first-stage filtering of input channels 0 through 7, respectively.
 - Jumpers W25 through W40 configure the second-stage filtering of input channels 0 through 7, respectively.
 - Jumper W41 directly connects the temperature sensor to the rear signal connector. To do so, set jumper W46 in the AB-R2 or AB-R0 position first.

Further configuration of the board is software controlled and will be discussed later in this chapter.

Digital Signal Connections

The four digital signal connection jumpers have position 1 marked on the board. Position 3 is not explicitly marked on the board.

The SCXI-1120 has three jumpers dedicated for communication between the data acquisition board and the SCXIbus. These jumpers are W42, W43, and W44.

Jumper W44

On Revision A and B modules, position 1 connects, after buffering, SLOTOSEL* to the SCXIbus INTR* line. This is the factory-default setting and should not be changed. In this setting, the data acquisition board controls the SCXIbus INTR* line. See the *Timing Requirements and Communication Protocol* section later in this chapter, and Chapter 5, *Programming*, for information on the use of the INTR* line. See Appendix E, *SCXI-1120 Cabling*, for the pin equivalences of the SCXI-1120 rear signal connector and the data acquisition board I/O connector.

Position 3 is reserved and should not be used.

On Revision C and later modules, jumper W44 is not loaded. SLOTOSEL* is always buffered to the INTR* line.

Jumper W43

Position 1 connects, after buffering, the SCXIbus MISO line to the SERDATOUT pin of the rear signal connector. In this setting, along with the proper setting of jumper W42, the data acquisition board can read the Module ID Register of the SCXI-1120. This is the factory-default setting. See the *Timing Requirements and Communication Protocol* section later in this chapter, and Chapter 4, *Register Descriptions*, for information on reading the Module ID Register. See Appendix E, *SCXI-1120 Cabling*, for the pin equivalences of the SCXI-1120 rear signal connector and the data acquisition board I/O connector.

Position 3 disconnects SERDATOUT from the SCXIbus MISO line.

Jumper W42

On Revision A and B modules, jumper W42 should not be connected. On Revision C and later modules, position 1 connects a 2.2 k Ω pullup resistor to the SERDATOUT line. Position 3 does not connect the pullup resistor to the SERDATOUT line.

Using Jumpers W42 and W43

If the SCXI-1120 is not cabled to a data acquisition board, the positions of these jumpers do not matter, so leave them in their factory-default positions (both in position 1).

If the SCXI-1120 is cabled to a data acquisition board, and the SCXI chassis that the SCXI-1120 is in, is the only SCXI chassis cabled to that data acquisition board, leave the jumpers in their factory-default positions (both in position 1).

If the SCXI-1120 is cabled to a data acquisition board, and there are multiple SCXI chassis cabled to that data acquisition board with shielded cables (you are using SCXI-1346 shielded cable multichassis adapters), leave the jumpers in their factory-default positions (both in position 1).

If the SCXI-1120 is cabled to a data acquisition board, and there are multiple SCXI chassis cabled to that data acquisition board with ribbon cables (you are using SCXI-1350 multichassis adapters), leave jumper W43 in its factory-default position (position 1). On all but one of the SCXI-1120s that are cabled to the data acquisition board, move jumper W42 to position 3. It does not matter which of the SCXI-1120 modules that are cabled to the data acquisition board has jumper W42 set to position 1. If you have different types of modules cabled to the data

acquisition board, those different modules will have jumpers similar to W43 and W42 of the SCXI-1120. Set those jumpers on the different modules using the same method described here for the SCXI-1120.

On Revision A and B SCXI-1120s, jumper W42 is not used. You set jumper W43 as explained in the cases above, except in the case of a multichassis ribbon cable system. In a multichassis ribbon cable system with Revision A and B SCXI-1120s cabled to the data acquisition board, you can access the MISO line in only one chassis. Pick one of the chassis that has the SCXI-1120 cabled to the DAQ board. Set jumper W43 on the SCXI-1120 to position 1. On the SCXI-1120s that are in the other chassis and cabled to the data acquisition board, set jumper W43 to position 3. Notice that you will only be able to access digital information from the chassis that has the SCXI-1120 with jumper W43 set to position 1.

On Revision C and later modules, the SERDATOUT line is driven with an open-collector driver (a driver that actively drives low or goes to a high-impedance state, relying on a pullup resistor to make the signal line go high). When using a single chassis, leave W42 and W43 in position 1, the factory default, on the SCXI-1120 that is connected to the data acquisition board. In this setting, the module drives MISO to SERDATOUT and connects the necessary pullup resistor to the SERDATOUT line. When using multiple chassis, leave jumper W43 in position 1 on all of the SCXI-1120s that are cabled to the data acquisition board. Only one of the SCXI-1120s that are cabled to the data acquisition board should have jumper W42 in position 1. It does not matter which of the SCXI-1120s that are cabled to the data acquisition board has the pullup connected. All of the other SCXI-1120 modules that are cabled to the data acquisition board should have jumper W42 in position 3. The reason for this is that if too many pullup resistors are attached to the SERDATOUT line, the drivers cannot drive the line low. See Table 2-1 for the description and configuration of the jumper settings.

Jumper	Description	Configuration
W42	Connects pullup to SERDATOUT (Revision C and later) factory- default setting.	3 • 2 1
W42	Parking position (not connected on Revision A and B)	3 2 1 •
W43	Connects MISO to SERDATOUT Factory-default setting.	
W43	Parking position	3 2 1 •

(continues)

Jumper	Description	Configuration
W45	Factory default	3 •
W44	Factory default (Revision A and B modules only)	
		1

Table 2-1.	Digital Signal	Connections, Jumper	Settings (Continued)
14010 - 11			

Analog Configuration

The SCXI-1120 has 42 analog configuration jumpers.

Before starting, notice that the jumper configurations for each channel are similar; only the jumper reference designator number changes. When you learn how to configure one channel, you can configure the other channels as well.

Grounding, Shielding, and Reference-Mode Selection

Jumper W46

Position B-R0R1 is the parked position and the factory-default setting.

Position AB-R0 connects the analog reference to the analog output ground (pins 1 and 2 on the rear signal connector). Select this configuration when using an RSE data acquisition board. You should not use differential input data acquisition boards when jumper W46 is in the AB-R0 position.

Position AB-R1 connects the analog reference to the SCXIbus guard.

Position AB-R2 enables the Pseudodifferential Reference mode and connects the analog reference to the OUTREF pin on the rear signal connector. Select this mode when the SCXI-1120 has to operate with data acquisition boards that have a nonreferenced single-ended input (NRSE). Do not use differential-input data acquisition boards when jumper W46 is in the AB-R2 position.

Note: The SCXI-1120 will drive pins 4, 6, 8, 10, 12, 14, 16, and 18 on the rear signal connector, although the SCXI-1120 is in pseudodifferential mode.

Jumper	Description	Configuration
W46	Factory setting in parking position	
W46	Connects the analog reference to AOGND (pins 1 and 2 of the rear signal connector). Use this connection with RSE data acquisition boards.	• • B • • A R2 R1 R0
W46	Connects SCXIbus guard to the analog reference	• • • B • • • A R2 R1 R0
W46	Enables the Pseudodifferential Reference mode (pin 19 of the rear signal connector is connected to the analog reference)	• • • B • • • A R2 R1 R0

Table 2-2. Jumper W46 Settings

Direct Temperature Connection

Jumper W41

When your SCXI-1120 is operating with a data acquisition board configured in a differential mode, such as the MIO board, you can access the temperature sensor only in the Multiplexed-Output mode. Direct temperature connection is not permissible to the data acquisition board. This is the factory setting and is position 1 of the jumper block. Position 3 is not explicitly marked.

If the temperature sensor needs to be accessed in parallel with the other eight outputs, or scanned–without software interference–along with the other channels, you need to place W41 in position 3 (this position is not explicitly marked on the module) and to configure your reference to pseudodifferential or single-ended operation (jumper W46) with your data acquisition board configured for the same reference scheme. In this position, the direct temperature sensor connection is made on pin 18 of the rear signal connector and corresponds to ACH15 of the MIO boards or the PC-LPM-16.

Jumper	Description	Configuration
W41	Temperature sensor accessed in MTS mode (Factory setting)	• 1 3 2 1
W41	Temperature sensor accessed in DTS mode, data acquisition board configured for NRSE or RSE	3 2 1

Table 2-3	Jumper	W41	Settings
1 doie 2 5.	Jumper	11 - 11	Dettings

Gain Jumpers

Each input channel has two gain stages. The first gain stage provides gains of 1, 10, 50, and 100, and the second stage provides gains of 1, 2, 5, 10, and 20. Tables 2-4 and 2-5 show how to set up the gain for each channel.

Input Channel Number	First Gain Jumper	Second Gain Jumper
0	W1	W9
1	W2	W10
2	W3	W11
3	W4	W12
4	W5	W13
5	W6	W14
6	W7	W15
7	W8	W16

Table 2-4.	Gain Jumper Allocation
------------	------------------------

The board is shipped with the first-stage gain set to 100 (position A), and a second-stage gain set to 10 (position D). To change the gain of your module, move the appropriate jumper on your module to the position indicated in Tables 2-3 and 2-4. Refer to Figure 2-1, *SCXI-1120 General Parts Locator Diagram*, and Figure 2-2, *Detailed Parts Locator Diagram*, for jumper locations on your module.

To determine the overall gain of a given channel use the following formula:

Overall gain = First-stage gain x second-stage gain.

Gain	Setting	Jumper Position
First-stage	1 10 50 100	D C B A (Factory setting)
Second-stage	1 2 5 10 20	A B C D (Factory setting) E

Filter Jumpers

Two-stage filtering is also available on your SCXI-1120 module. The first stage is located in the isolated section of the input channel, whereas the second stage is located in the nonisolated section of your input channel. Two-stage filtering eliminates the noise generated by the isolation amplifier, producing a higher signal-to-noise ratio. Furthermore, two filter bandwidths are available, 10 kHz and 4 Hz.

Input Channel	First Filter Jumper		Second Filter Jumper		
Number	4 Hz (Factory Setting)	10 kHz	4 Hz (Factory Setting)	10 kHz	
0	W17-A	W17-B	W25	W26	
1	W18-A	W18-B	W27	W28	
2	W19-A	W19-B	W29	W30	
3	W20-A	W20-B	W31	W32	
4	W21-A	W21-B	W33	W34	
5	W22-A	W22-B	W35	W36	
6	W23-A	W23-B	W37	W38	
7	W24-A	W24-B	W39	W40	

Table 2-6. Filter Jumper Allocation

Your SCXI-1120 is shipped in the 4 Hz position. Remember to make sure that both stages are set to the same bandwidth to ensure that the required bandwidth is achieved. Notice that one jumper block is available for each filter stage.

Hardware Installation

You can install the SCXI-1120 in any available SCXI chassis. After you have made any necessary changes and have verified and recorded the jumper settings on the form in Appendix G, *Customer Communication*, you are ready to install the SCXI-1120. The following are general installation instructions, but consult the user manual or technical reference manual of your SCXI chassis for specific instructions and warnings.

- 1. Turn off the computer that contains the data acquisition board or disconnect it from your SCXI chassis.
- 2. Turn off the SCXI chassis. Do not insert the SCXI-1120 into a chassis that is turned on.
- 3. Insert the SCXI-1120 into the module guides. Gently guide the module into the back of the slot until the connectors make good contact. If a cable assembly has already been installed in the rear of the chassis, the module and cable assembly must be firmly engaged; however, do not *force* the module into place.
- 4. Screw the front mounting panel of the SCXI-1120 to the top and bottom threaded strips of your SCXI chassis.
- 5. If this module is to be connected to an MIO-16 data acquisition board, attach the connector at the metal end of the SCXI-1340 cable assembly to the rear signal connector on the SCXI-1120 module. Screw the rear panel to the rear threaded strip. Attach the loose end of the cable to the MIO-16 board.
 - **Note:** For installation procedures with other SCXI accessories and data acquisition boards, consult Appendix E, *SCXI-1120 Cabling*.
- 6. Check the installation.
- 7. Turn on the SCXI chassis.
- 8. Turn on the computer or reconnect it to your chassis.

The SCXI-1120 board is installed and ready for operation.

Signal Connections

This section describes the input and output signal connections to the SCXI-1120 board via the SCXI-1120 front connector and rear signal connector, and includes specifications and connection instructions for the signals given on the SCXI-1120 connectors.

Warning: Connections that exceed any of the maximum ratings of input or output signals on the SCXI-1120 can result in damage to the SCXI-1120 board and to the SCXIbus. Maximum input ratings for each signal are given in this chapter under the discussion of that signal. National Instruments is *not* liable for any damages resulting from such signal connections.

Front Connector

Pin Number	Signal Name	A	ł	Column B C		Signal Name
		Г			1	
32	CH0+	+	-0	<u> </u>	\vdash	CH0-
31			0	0		
30	CH1+	+	-0	~	\vdash	CH1-
29			0	0		
28			0	0		
27			0	0		
26	CH2+	+	-0	<u> </u>	\vdash	CH2-
25			0	0		
24	CH3+	+	-0	<u> </u>	\vdash	CH3-
23			0	0		
22			0	0		
21			0	0		
20	CH4+	+	-0	0 —	\vdash	CH4-
19			0	0		
18	CH5+	+	-0	~	\vdash	CH5-
17			0	0		
16			0	0		
15			0	0		
14	CH6+	+	-0	<u> </u>	\vdash	CH6-
13			0	0		
12	CH7+	+	-0	<u> </u>	\vdash	CH7-
11			0	0		
10			0	0		
9			0	0		
8			0	<u> </u>	\vdash	RSVD
7			0	0		
6	RSVD	+	-0	<u> </u>	\vdash	RSVD
5			0	0		
4	+5 V	+	-0	~	\vdash	MTEMP
3			0	0		
2	CHSGND	+	-0	<u> </u>	\vdash	DTEMP
1			0	0		

Figure 2-3 shows the pin assignments for the SCXI-1120 front connector.

Figure 2-3. SCXI-1120 Front Connector Pin Assignment

Front Connector Signal Descriptions

Pin	Signal Name	Description
A2	CHSGND	Chassis Ground – Tied to the SCXI chassis.
C2	DTEMP	Direct Temperature Sensor – Connects the temperature sensor to pin 18 of the rear signal connector MCH7- when the terminal block is configured for direct temperature connection and jumper W41 is in position 3.
A4	+5 V	+5 VDC Source – Used to power the temperature sensor on the terminal block. 0.2 mA of source not protected.
C4	МТЕМР	Multiplexed Temperature Sensor – Connects the temperature sensor to the output multiplexer.
A6, C6, C8	RSVD	Reserved – Reserved for future use. Do not connect any signals to these pins. TTL/CMOS output. They are not protected.
A8, A10, C10, A16, C16,A22, C22, A28, C28	No Connect	Do not connect any signals to these pins.
A12, A14, A18, A26, A20, A24, A30, A32	CH7+ through CH0+	Positive Input Channels – The positive inputs to channels 7 through 0, respectively.
C12, C14, C18, C20, C24, C26, C30, C32	CH7- through CH0-	Negative Input Channels – The negative inputs to channels 7 through 0, respectively.

The signals on the front connector are all analog with the exceptions of pins A6, C6, and C8. The analog signals can be divided into two groups—the analog input channels, and the temperature sensor.

Analog Input Channels

The positive input channels are located in column A. Their corresponding negative input channels are located in column C. Each input corresponds to a separate amplifier and is fully isolated from the other channels and from earth ground. The inputs are designed in a floating single-ended configuration, thus the measured signal can be referenced to a ground level with common-mode voltage up to 250 Vrms. For better noise immunity, connect the negative input channel to the signal reference. If the measured signals are floating, connect the negative input channel to chassis ground on the terminal block. Figure 2-4 shows how to connect a ground-referenced signal. Figure 2-5 shows how to connect a floating signal. Figures 2-6 and 2-7 show how to connect AC-coupled signals.



Figure 2-4. Ground-Referenced Signal Connection with High Common-Mode Voltage



Figure 2-5. Floating Signal Connection Referenced to Chassis Ground for Better Signal-to-Noise Ratio



Figure 2-6. Floating AC-Coupled Signal Connection



Figure 2-7. AC-Coupled Signal Connection with High Common-Mode Voltage

For AC-coupled signals, an external resistor from the positive input channel to the signal reference should be connected. This is needed to provide the DC path for the positive input bias current. Typical resistor values range from $100 \text{ k}\Omega$ to $1 \text{ M}\Omega$. This solution, although necessary in this case, lowers the input impedance of the input channel amplifier and introduces an additional offset voltage proportional to the input bias current and to the resistor value used. The typical input bias current of the amplifier consists of $\pm 80 \text{ pA}$ and a negligible offset drift current. When a 100 k Ω resistor is used, this will result into $\pm 8 \mu V$ of offset, which is insignificant in most applications. However, if larger valued bias resistors are used, significant input offset may result. To determine the maximum offset introduced by the biasing resistor, use the following equation:

 $V_{ofsbias} = I_{bias} \times R_{bias}$

The input signal range of an SCXI-1120 input channel is ± 5 V/G_{total} referenced to its negative input, where G_{total} is equal to the product of the first-stage and second-stage gains. In addition, the input channels are overvoltage protected to 240 Vrms with power on or off at a maximum of 4.5 mArms sink or source.

Warning: Exceeding the input signal range and the common-mode input range results in distorted signals. Exceeding the maximum input voltage rating (250 Vrms between terminals, and between any terminal and ground) can result in damage to the SCXI-1120, the SCXIbus, and the data acquisition board. National Instruments is *not* liable for any damages resulting from such signal connections.

Temperature Sensor Connection

Pins C2 and C4 are dedicated for connecting the temperature sensor to the SCXI-1120. The temperature sensor is not isolated and is referenced to the chassis ground. The connection is overvoltage protected to ± 25 VDC with power on and ± 15 VDC with power off.

Warning: Exceeding the overvoltage protection on the temperature connections can result in damage to the SCXI-1120, the SCXIbus, and the data acquisition board. National Instruments is *not* liable for any damages resulting from such signal connections.

Connector-and-Shell Assembly

Two types of signal connectors are available to connect the signals to the SCXI-1120 inputs. The first, the SCXI-1330 32-pin DIN C female connector-and-shell assembly, is available in a kit listed in the *Optional Equipment* section in Chapter 1, *Introduction*. The connector has eyelet ends for easy hook-and-solder wire connection. With this kit, you can build your own signal cable to connect to the SCXI-1120 inputs. After you have built the cable, the shell covers and protects the connector. Perform the following steps to assemble and mount the connector-and-shell assembly to your SCXI module:

- 1. Refer to Figure 2-8, *Assembling and Mounting the SCXI-1330 Connector-and-Shell Assembly*, and the diagram included with your SCXI-1330 kit to build the connector-and-shell assembly.
- 2. Turn off the computer that contains your data acquisition board or disconnect the board from your SCXI chassis.
- 3. Turn off your SCXI chassis.
- 4. Slide the selected module out of the SCXI chassis.
- 5. Remove the module cover.
- 6. Place one jack screw as indicated in Figure 2-8.
- 7. While holding the jack screw in place, insert the lock washer and then the nut. Notice that you might need long-nose pliers to insert the washer and nut.
- 8. Tighten the nut by holding it firmly and rotating the jack screw.
- 9. Repeat steps 6 through 8 for the second jack screw.
- 10. Replace the module cover and tighten the grounding screw.
- 11. Slide the module back in place.
- 12. Connect the SCXI-1330 to your module connector and secure it by tightening both mounting screws.



Figure 2-8. Assembling and Mounting the SCXI-1330 Connector-and-Shell Assembly

SCXI-1320 and SCXI-1328 Terminal Blocks

The second type of connector available to connect the signals to the SCXI-1120 inputs is a terminal block with an onboard temperature sensor and screw terminals for easy connection. One terminal block, the SCXI-1328 isothermal terminal block, has a high-accuracy onboard temperature sensor. The terminal block kits are listed in the *Optional Equipment* section in Chapter 1, *Introduction*.

The SCXI-1320 terminal block and SCXI-1328 high-accuracy isothermal terminal block consist of a shielded board with supports for connection to the SCXI-1120 input connector. The terminal blocks have 18 screw terminals for easy connection. Eight pairs of screw terminals are for signal connection to the eight inputs of the SCXI-1120, and one pair of screw terminals connects to the chassis ground.

The following warnings contain important safety information concerning hazardous voltages and terminal blocks.

Warnings: When using the terminal block with high common-mode voltages, you *must* insulate your signal wires appropriately. National Instruments is *not* liable for any damages or injuries resulting from inadequate signal wire insulation.

If high voltages (\geq 42 Vrms) are present, *you must connect the safety earth ground to the strain-relief tab*. This complies with UL 1244 and protects against electric shock when the terminal block is not connected to the chassis. To connect the safety earth ground to the strain-relief tab, run an earth ground wire in the cable from the signal source to the terminal block. National Instruments is *not* liable for any damages or injuries resulting from inadequate safety earth ground connections.

When connecting your signals to the SCXI-1320 terminal block for use with the SCXI-1120, follow the labeling on the SCXI-1320 indicated under the module type column for the SCXI-1120 as indicated in Figure 2-9.

When connecting your signals to the SCXI-1328 high-accuracy isothermal terminal block for use with the SCXI-1120, follow the labeling on the SCXI-1328 indicated along the module type row for the SCXI-1120 as indicated in Figure 2-10.

Terminal Block Temperature Sensor

To accommodate thermocouples with the SCXI-1120, the terminal block has a temperature sensor for cold-junction compensation. You can connect the temperature sensor in two ways:

- You can connect the temperature sensor to the MTEMP pin (C4) on the module front connector and multiplex the sensor at the output multiplexer along with amplifier outputs. This is the Multiplexed Temperature Sensor (MTS) mode. Refer to the *Configuration Register* section in Chapter 4, *Register Descriptions*, for further details.
- You can connect the temperature sensor to a separate data acquisition channel via pin 18 on the module rear signal connector when you set SCXI-1120 jumper W41 to position 3. This is the Direct Temperature Sensor (DTS) mode.
- **Note:** Use an average of a large number of samples to obtain the most accurate reading. Noisy environments require more samples for greater accuracy.

The SCXI-1320 temperature sensor outputs 10 mV/°C and has an accuracy of $\pm 1^{\circ}$ C over the 0° to 55° C temperature range. To determine the temperature, use the following formulas:

$$T(^{\circ}C) = 100(V_{\text{TEMPOUT}})$$

T (°F) =
$$\frac{[T (°C)] 9}{5} + 32$$

where V_{TEMPOUT} is the temperature sensor output and T (°F) and T (°C) are the temperature readings in degrees Fahrenheit and degrees Celsius, respectively.

The SCXI-1328 temperature sensor outputs 0.62 to 0.07 V from 0° to 55° C and has an accuracy of $\pm 0.35^{\circ}$ C over the 15° to 35° C range and $\pm 0.65^{\circ}$ C over the 0° to 15° and 35° to 55° C ranges.

To determine the temperature, use the following formulas:

 $T(^{\circ}C) = T = T_{K} - 273.15$

where T_K is the temperature in kelvin

$$\begin{split} T_{\rm K} &= \frac{1}{\left[a + b \left(\ln R_{\rm T} \right) + c \left(\ln R_{\rm T} \right)^3 \right]} \\ a &= 1.288 \ \text{x} \ 10^{-3} \\ b &= 2.356 \ \text{x} \ 10^{-4} \\ c &= 9.556 \ \text{x} \ 10^{-8} \\ R_{\rm T} &= \text{resistance of the thermistor in } \Omega \end{split}$$

$$R_{T} = 50,000 \left(\frac{V_{TEMPOUT}}{2.5 - V_{TEMPOUT}} \right)$$

 V_{TEMPOUT} = output voltage of the temperature sensor

T (°F) =
$$\frac{[T (°C)] 9}{5} + 32$$

where T (°F) and T (°C) are the temperature readings in degrees Fahrenheit and degrees Celsius, respectively.

Terminal Block Jumper Configuration

In addition to the screw terminals, the terminal block has one jumper for configuring the onboard temperature sensor. When you set jumper W1 on the terminal block to the MTEMP position, the jumper connects the temperature sensor to the SCXI-1120 output multiplexer. This is the factory setting. The DTEMP position connects the temperature sensor to SCXI-1120 jumper W41.

In both MTS and DTS modes, the reference to the temperature sensor signal is the SCXI-1120 analog ground that is connected to MCHO- in the MTS mode, or to OUTREF or AOGND (with SCXI-1120 jumper W46 set in positions AB-R2 and AB-R0, respectively) in the DTS mode.

One jumper block comprises both positions; thus, you can use only one type of configuration at a time. The parking position for the jumper block is the MTEMP position (the temperature sensor is disabled until the RTEMP bit in the Configuration Register selects the sensor).

Tables 2-7 and 2-8 show the jumper settings on the SCXI-1320 and SCXI-1328 terminal blocks.

Jumper	Position	Description
W1 W1	MTEMP••••MTEMP••DTEMPDTEMP	MTS mode selected; factory setting; parking position DTS mode selected

 Table 2-7. Jumper Settings on the SCXI-1320 Terminal Block

Jumper	Position	Description
W1	DTEMP . MTEMP	MTS mode selected; factory setting; parking position
W1	DTEMP . MTEMP	DTS mode selected

Table 2-8. Jumper Settings on the SCXI-1328 Terminal Block

Terminal Block Signal Connection

Warnings: The chassis GND terminals on your terminal block are for grounding high impedance sources such as a floating source (1 mA maximum). Do *not* use these terminals as safety earth grounds.

If high voltages (\geq 42 Vrms) are present, *you must connect the safety earth ground to the strain-relief tab*. This complies with UL 1244 and protects against electric shock when the terminal block is not connected to the chassis. To connect the safety earth ground to the strain-relief tab, run an earth ground wire in the cable from the signal source to the terminal block. National Instruments is *not* liable for any damages or injuries resulting from inadequate safety earth ground connections.



Shock Hazard: This unit should only be opened by qualified personnel aware of the dangers involved. Disconnect all power before removing cover. Always install grounding screw.

To connect the signal to the terminal block, use the following procedure:

- 1. Remove the grounding screw of the top cover.
- 2. Snap out the top cover of the shield by placing a screwdriver in the groove at the bottom of the terminal block.
- 3. Slide the signal wires, one at a time, through the front panel strain-relief opening. You can add insulation or padding if necessary.
- 4. Connect the wires to the screw terminals by wrapping the wires around the screws and tightening the screws without letting the wires slip out.
- 5. Tighten the larger strain-relief screws.
- 6. Snap the top cover back in place.
- 7. Reinsert the grounding screw to ensure proper shielding.
- 8. Connect the terminal block to the SCXI-1120 front connector as explained in the *Terminal Block Installation* section later in this chapter.

Figure 2-9 shows a parts locator diagram for the SCXI-1320 terminal block. Figure 2-10 shows a parts locator diagram for the SCXI-1328 terminal block.
Figure 2-9. SCXI-1320 Parts Locator Diagram

Figure 2-10. SCXI-1328 Parts Locator Diagram

Terminal Block Installation

To connect the terminal block to the SCXI-1120 front connector, perform the following steps:

- 1. Connect the SCXI-1120 front connector to its mating connector on the terminal block.
- 2. Make sure that the SCXI-1120 top and bottom thumbscrews do not obstruct the rear panel of the terminal block.
- 3. Tighten the top and bottom screws on the back of the terminal block to hold it securely in place.

Rear Signal Connector

Note: If you will be using the SCXI-1120 with a National Instruments data acquisition board and cable assembly, you do not need to read the remainder of this chapter. If you will also be using the SCXI-1180 feedthrough panel, the SCXI-1343 rear screw terminal adapter, or the SCXI-1351 one-slot cable extender with the SCXI-1120, you should read this section.

Figure 2-11 shows the pin assignments for the SCXI-1120 rear signal connector.



Figure 2-11. SCXI-1120 Rear Signal Connector Pin Assignment

Rear Signal Connector Signal Descriptions

Pin	Signal Name	Description
1-2	AOGND	Analog Output Ground – Connected to the analog reference when jumper W46 is in position AB-R0.
3-18	MCH0± through MCH7±	Analog Output Channels 0 through 7 – Connects to the data acquisition board differential analog input channels.
19	OUTREF	Output Reference – Serves as the reference node for the analog output channels and the temperature sensor–in the DTS mode–in the Pseudodifferential Reference mode. It should be connected to the analog input sense of the NRSE data acquisition board.
24, 33	DIG GND	Digital Ground – Supply the reference for data acquisition board digital signals and are tied to the module digital ground.
25	SERDATIN	Serial Data In – Taps into the SCXIbus MOSI line to provide serial input data to a module or Slot 0.
26	SERDATOUT	Serial Data Out – Taps into the SCXIbus MISO line to accept serial output data from a module.
27	DAQD*/A	Data Acquisition Board Data/Address Line – Taps into the SCXIbus D*/A line to indicate to the module whether the incoming serial stream is data or address information.
29	SLOT0SEL*	Slot 0 Select – Taps into the SCXIbus INTR* line to indicate whether the information on MOSI is being sent to a module or Slot 0.
36	SCANCLK	Scan Clock – Indicates to the SCXI-1120 that a sample has been taken by the data acquisition board and causes the SCXI-1120 to change channels.
37	SERCLK	Serial Clock – This signal taps into the SCXIbus SPICLK line to clock the data on the MOSI and MISO lines.
43	RSVD	Reserved.

All other pins are not connected.

See the *Timing Requirements and Communication Protocol* section later in this chapter for more detailed information on timing.

The signals on the rear signal connector can be classified as analog output signals, digital I/O signals, or timing I/O signals. Signal connection guidelines for each of these groups are given in the following section.

Analog Output Signal Connections

Pins 1 through 19 of the rear signal connector are analog output signal pins. Pins 1 and 2 are AOGND signal pins. AOGND is an analog output common signal that is routed through jumper W46 to the analog reference on the SCXI-1120. You can use these pins for a general analog power ground tie point to the SCXI-1120 if necessary. In particular, when using differential input data acquisition boards, such as the MIO-16 board, it is preferable to leave jumper W46 in its factory setting or in position AB-R1 to avoid ground loops. With data acquisition boards that are configured for referenced single-ended (RSE) measurements, jumper W46 should be in position AB-R0 to connect the SCXI-1120 analog ground reference to the data acquisition analog ground. Pin 19 is the OUTREF pin, and is connected internally to the analog reference when jumper W46 is in position AB-R2. Pins 3 through 18 are the analog output channels of the SCXI-1120. Pins 3 and 4, or MCH0±, are a multiplexed output of all eight channels and the temperature sensor output. Pins 5 through 18, or MCH1± through MCH7±, are a parallel connection of channels 1 through 7 to the rear signal connector. Pin 18 is a direct connection to the temperature sensor when jumper W41 is in position 3. Notice that the temperature sensor is located on the terminal block. For further details on configuring the temperature sensor output, refer to the SCXI-1320 and SCXI-1328 Terminal Blocks section earlier in this chapter.

Warning: The SCXI-1120 analog outputs are *not* overvoltage protected. Applying external voltage to these outputs can result in damage to the SCXI-1120. National Instruments is *not* liable for any damages resulting from such signal connections.

Note: The SCXI-1120 analog outputs are short-circuit protected.

Digital I/O Signal Connections

Pins 24 through 27, 29, 33, 36, 37, and 43 constitute the digital I/O lines of the rear signal connector. They are divided into three categories—the digital input signals, the digital output signals, and the digital timing signals.

The digital input signals are pins 24, 25, 27, 29, 33, and 37. The data acquisition board uses these pins to configure the SCXI module that is under data acquisition board control. Each digital line emulates the SCXIbus communication signals as follows:

- Pin 25 is SERDATIN and is equivalent to the SCXIbus MOSI serial data input line.
- Pin 27 is DAQD*/A and is equivalent to the SCXIbus D*/A line. It indicates to the module whether the incoming serial stream on SERDATIN is data (DAQD*/A = 0) or address (DAQD*/A = 1) information.
- Pin 29 is SLOT0SEL* and is equivalent to the SCXIbus INTR* line. It indicates whether the data on the SERDATIN line is being sent to Slot 0 (SLOT0SEL* = 0) or to a module (SLOT0SEL* = 1).
- Pins 24 and 33 are the digital ground references for the data acquisition board digital signals and are tied to the module digital ground.
- Pin 37 is SERCLK and is equivalent to the SCXIbus SPICLK line and is used to clock the serial data on the SERDATIN line into the module registers.

The digital output signal is pin 26:

• Pin 26 is SERDATOUT and is equivalent to SCXIbus MISO when jumper W43 is in position 1.

The digital I/O signals of the SCXI-1120 match the digital I/O lines of the MIO-16 board. When used with an SCXI-1341, SCXI-1342, or SCXI-1344 cable assembly, the SCXI-1120 signals match the digital lines of the Lab-NB/Lab-PC+/Lab-LC boards and the PC-LPM-16 board, respectively. Table 2-9 lists the equivalences. For more information, consult Appendix E, *SCXI-1120 Cabling*.

SCXIbus Line	SCXI-1120 Rear Signal Connector	MIO-16 Board	Lab-NB/Lab-PC/ Lab-PC+/Lab-LC	PC-LPM-16
MOSI	SERDATIN	ADIO0	PB4	DOUT4
D*/A	DAQD*/A	ADIO1	PB5	DOUT5
INTR*	SLOT0SEL*	ADIO2	PB6	DOUT6
SPICLK	SERCLK	EXTSTROBE*	PB7	DOUT7
MISO	SERDATOUT	BDIO0	PC1	DIN6

Table 2-9. SCXIbus to SCXI-1120 Rear Signal Connector toData Acquisition Board Pin Equivalences

The digital timing signals are pins 36 and 43:

- Pin 36 is used as a clock by the SCXI-1120 to increment the MUXCOUNTER after each conversion by the data acquisition board during scanning. This signal is referred to as SCANCLK. See Chapter 3, *Theory of Operation*, for a description of MUXCOUNTER.
- Pin 43 is a reserved digital input.

The following specifications and ratings apply to the digital I/O lines.

Absolute maximum voltage	
input rating	5.5 V with respect to DIG GND

Digital input specifications (referenced to DIG GND):

V _{IH} input logic high voltage	2 V minimum
V _{IL} input logic low voltage	0.8 V maximum

 I_I input current leakage $\pm 1 \ \mu A$ maximum

Digital output specifications (referenced to DIG GND):

V _{OH} output logic high voltage	3.7 V minimum at 4 mA maximum
V _{OL} output logic low voltage	0.4 V maximum at 4 mA maximum

Timing Requirements and Communication Protocol

Timing Signal

The data acquisition timing signal is SCANCLK.

SCANCLK is used to increment MUXCOUNTER on its rising edge. Figure 2-12 shows the timing requirements of the SCANCLK signal. These requirements will ensure that SCANCLK is properly transmitted over TRIG0.



Figure 2-12. SCANCLK Timing Requirements

For output selection time specifications, refer to Appendix A, Specifications.

Communication Signals

This section describes the methods for communicating on the Serial Peripheral Interface (SPI) bus and their timing requirements. The communication signals are SERDATIN, DAQD*/A, SLOT0SEL*, SERDATOUT, and SERCLK. Furthermore, SS* is produced by Slot 0 according to data acquisition board programming, and SS* timing relationships will also be discussed. For information on the Slot 0 Slot-Select Register, consult Chapter 4, *Register Descriptions*.

The data acquisition board determines to which slot it will talk by writing a slot-select number to Slot 0. In the case of an SCXI-1001 chassis, this write also determines to which chassis the data acquisition board will talk. Writing a slot-select number is also used in programming the Slot 0 hardscan circuitry. See Chapter 5, *Programming*, for information on programming the Slot 0 hardscan circuitry.

The following sections detail the procedure for selecting a slot in a particular chassis. Figure 2-13 illustrates the timing of this procedure with the example case of selecting Slot 11 in Chassis 9. Notice that the factory-default chassis address for the SCXI-1000 is address 0. For information on changing the address of your chassis, consult the *SCXI-1000/1001 User Manual*. An SCXI-1000 chassis will respond to any chassis number.



Figure 2-13. Slot-Select Timing Diagram

To write the 16-bit slot-select number to Slot 0, follow these steps:

1. Initial conditions:

SERDATIN = don't care. DAQD*/A = don't care. SLOT0SEL* = 1. SERCLK = 1.

- 2. Clear SLOTOSEL* to 0. This will deassert all SS* lines to all modules in all chassis.
- 3. For each bit, starting with the MSB, perform the following action:
 - a. SERDATIN = bit to be sent. These bits are the data that are being written to the Slot-Select Register.
 - b. SERCLK = 0.
 - c. SERCLK = 1. This rising edge clocks the data.
- 4. Set SLOT0SEL* to 1. This will assert the SS* line of the module whose slot number was written to Slot 0. If multiple chassis are being used, only the appropriate slot in the chassis whose address corresponds to the written chassis number will be selected. When no communication is taking place between the data acquisition board and any modules, you should write zero to the Slot-Select Register to ensure that no accidental writes occur.

Figure 2-14 shows the timing requirements on the SERCLK and SERDATIN signals. You must observe these timing requirements for all communications. T_{delay} is a specification of the SCXI-1120.



Figure 2-14. Serial Data Timing Diagram

After the Slot-Select line to an SCXI-1120 has been asserted, you can write to its Configuration Register and read from its Module ID Register using the following protocols. The contents of the Module ID Register are reinitialized by deasserting Slot-Select. After the 32 bits of data are read from the Module ID Register, further data will be zeros until reinitialization occurs.

To write to the Configuration Register, follow these steps:

1. Initial conditions:

SS* asserted low. SERDATIN = don't care. DAQD*/A = 0 (indicates data will be written to Configuration Register). SLOT0SEL* = 1. SERCLK = 1 (and has not transitioned since SS* went low).

2. For each bit to be written:

Establish the desired SERDATIN level corresponding to this bit. SERCLK = 0.SERCLK = 1. Clock the data.

- 3. Pull SLOT0SEL* low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.
- 4. If you are not selecting another slot, you should write zero to the Slot 0 Slot-Select Register.

Figure 2-15 illustrates a write to the SCXI-1120 Configuration Register of the binary pattern:

10000011 00001111



Figure 2-15. Configuration Register Write Timing Diagram

To read from the Module ID Register, follow these steps:

1. Initial conditions:

SS* asserted low. SERDATIN = don't care. DAQD*/A = 1. Make sure DAQD*/A does not go low or erroneous data will be written to the Configuration Register. SLOT0SEL* = 1. SERCLK = 1 (and has not changed since SS* went low).

2. For each bit to be read:

SERCLK = 0. SERCLK = 1. Clock the data. Read the level of the SERDATOUT line.

- 3. Pull SLOT0SEL* low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.
- 4. If you are not selecting another slot, you should write zero to the Slot 0 Slot-Select Register.

Figure 2-16 illustrates a read of the SCXI-1120 Module ID Register.





For further details on programming these signals, refer to Chapter 5, Programming.

Chapter 3 Theory of Operation

This chapter contains a functional overview of the SCXI-1120 module and explains the operation of each functional unit making up the SCXI-1120.

Functional Overview

The block diagram in Figure 3-1 illustrates the key functional components of the SCXI-1120.



Figure 3-1. SCXI-1120 Block Diagram

The major components of the SCXI-1120 are as follows:

- SCXIbus connector
- Digital interface
- Digital control circuitry
- Timing and analog circuitry

The SCXI-1120 consists of eight isolated amplifier channels with gains of 1, 2, 5, 10, 20, 50, 100, 200, 500, 1,000, and 2,000. The SCXI-1120 also has a digital section for automatic control of channel scanning, temperature selection, and MUXCOUNTER clock selection.

The theory of operation of each of these components is explained in the rest of this chapter.

SCXIbus Connector

Figure 3-2 shows the pinout of the SCXIbus connector.

			
GUARD	A1 o o	0 0 D1	GUARD
GUARD	B1 0 0	C1	GUARD
GUARD	A2	D2	GUARD
AB0+	B2 0 0	C2	AB0-
GUARD	A3	D3	GUARD
GUARD	B3 0 0	C_{3}	GUARD
GUARD	A4	D4	GUARD
ooning	B4 0 0	\circ \circ $C4$	Corne
GUARD	A5	D5	GUARD
GUARD		\circ \circ C_5	GUARD
GUARD	A6	D6	GUARD
GOIRD		\circ \circ C_{6}	GUIRD
	<u> </u>	D7	
		$\circ \circ \frac{D7}{C7}$	
	D7		
		$\varphi \circ \frac{D_0}{C_0^8}$	
		$\circ \circ \frac{D9}{C0}$	
	B9	<u> </u>	
		$\circ \circ \frac{D10}{C10}$	
	B10	<u>C10</u>	
		o o <u>D11</u>	
	B11	C11	
	A12 0 0	o o <u>D12</u>	
	B12	C12	
	A13 0	0 0 D13	
	B13	C13	CHSGND
	A14 0 0	$D = \frac{D14}{D14}$	
	B14	C14	CHSGND
	A15 0 0	0 0 D15	
	B15	C15	CHSGND
	A16	D16	
	B16 J	C16	CHSGND
	A17 0 0	D17	
	B17 0 0	C17	CHSGND
	A18	D18	
	B18 0	C18	RSVD
RESET*	A19	D19	INTR*
MISO	B19 0	C19	D*/A
V-	A20	D20	V-
<u>V-</u>	B20 0 0	\circ \circ $C20$	V-
CHSGND	A21	D21	CHSGND
CHSGND	B21 0 0	\circ \circ $\frac{D21}{C21}$	CHSGND
	A22		V+
	B22 0 9	\circ \circ $\frac{D22}{C22}$	v T V+
	Δ22 Δ23		<u>v</u> +
	A23 P22 Q	$\varphi \circ \frac{D23}{C22}$	
TRICO	D23		MOSI
	A24 D24 0 Q	ο ο <u>D24</u>	COANCON
99. _*	B24	L C24	SCANCON
	L		

Figure 3-2. SCXIbus Connector Pin Assignment

SCXIbus Connector Signal Descriptions

Pin	Signal Name	Description	
A1, B1, C1, D1, A2, D2, A3, B3, C3, D3, A4, D4, A5, B5, C5, D5, A6, D6	GUARD	Guard – Shields and guards the analog bus lines from noise.	
B2	AB0+	Analog Bus 0+ – Positive analog bus 0 line. Used to multiplex several modules to one analog signal.	
C2	AB0-	Analog Bus 0- – Negative analog bus 0 line. Used to multiplex several modules to one analog signal.	
C13-C17, A21, B21, C21, D21	CHSGND	Chassis Ground – Digital and analog ground reference.	
C18	RSVD	Reserved.	
A19	RESET*	Reset – When pulled low, reinitializes the module to its power-up state. Totem pole. Input.	
B19	MISO	Master-In-Slave-Out – Transmits data from the module to the SCXIbus. Open collector. I/O.	
C19	D*/A	Data/Address – Indicates to the module whether address information or data information is being sent to the module on MOSI. Open collector. I/O.	
D19	INTR*	Interrupt – Active low. Causes data that is on MOSI to be written to the Slot-Select Register Slot 0. Open collector. Output.	
A20, B20, C20, D20	V-	Negative Analog Supply – -18.5 V to -25 V.	
A22, B22, C22, D22	V+	Positive Analog Supply – +18.5 V to +25 V.	
A23, D23	+5 V	+5 VDC Source – Digital power supply.	
B23	SPICLK	Serial Peripheral Interface (SPI) Clock – Clocks the serial data on the MOSI and MISO lines. Open collector. I/O.	
C23	MOSI	Master-Out-Slave-In – Transmits data from the SCXIbus to the module. Open collector. I/O.	

Pin	Signal Name	Description (continued)
A24	TRIG0	TRIG0 – General-purpose trigger line used by the SCXI-1120 to send SCANCLK to other modules or receive SCANCLK from other modules. Open collector. I/O.
B24	SS*	Slot Select – When low, enables module communications over the SCXIbus. Totem pole. Input.
C24	SCANCON	Scanning Control – Combination output enable and reload signal for scanning operations. Totem pole. Input.

All other pins are not connected.

MOSI, MISO, SPICLK, and SS* form a synchronous communication link that conforms with SPI using an idle-high clock and second-edge data latching. D*/A, INTR*, and RESET* are additional control signals.

When the module is being used in an SCXI-1000 or SCXI-1001 chassis, the data acquisition board, via the module rear signal connector, must tap into the open-collector backplane signal lines as a master to write to the module. The signal connections from the rear signal connector to the backplane are shown in Table 3-1.

Table 3-1.	SCXIbus	Equivalents	for the	Rear Signal	Connector
14010 0 11	001110000		101 0110	- com ~ Build	001110000

Rear Signal Connector Signal	SCXIbus Equivalent	
SERDATIN DAQD*/A SLOT0SEL*	MOSI D*/A INTR*	Jumper W44 must be set to position 1
SERCLK SERDATOUT	SPICLK MISO	(Revision A and B modules only) Jumper 43 must be set to position 1

The SCXI-1120 module converts the data acquisition board signals to open-collector signals on the backplane of the SCXI chassis. In order for the data acquisition board to talk to a slot, the board must first assert the SS* for that slot. This is done by asserting INTR* low, writing a 16-bit number over MOSI corresponding to the desired slot (and chassis if an SCXI-1001 chassis is being used), and then releasing INTR* high. At this point, the SS* of the desired slot is asserted low and the data acquisition board can communicate with the module in that slot according to the SPI protocol.

Digital Interface



Figure 3-3 shows a diagram of the SCXI-1120 and SCXIbus digital interface circuitry.

Figure 3-3. Digital Interface Circuitry Block Diagram

The digital interface circuitry is divided into a data acquisition section and an SCXIbus section. The SCXI-1120 connects to the SCXIbus via a 4x24 metral receptacle and to the data acquisition board via a 50-pin ribbon-cable header. The digital interface circuitry buffers the digital signals from the data acquisition board and the SCXIbus and sends signals back and forth between the data acquisition board and the SCXIbus.

Digital Control Circuitry

Figure 3-4 diagrams the SCXI-1120 digital control.



Figure 3-4. SCXI-1120 Digital Control

The digital control section consists of the Configuration Register and the Module ID Register.

The Configuration Register is a two-byte, serial-in, parallel-out shift register. Data is received on the MOSI line from either Slot 0 or the data acquisition board when SS* is enabled and D*/A indicates data transfer (D*/A low). The Configuration Register provides channel selection and configures the SCXI-1120 for scanning options. All the control bits are fed into a latch before being routed to the rest of the module. The channel-select bits are taken directly from the shift register. Complete descriptions of the register bits are given in Chapter 4, *Register Descriptions*. Writes to the Configuration Register require the following steps:

- 1. SS* goes low, enabling communication with the board.
- 2. D*/A goes low, indicating that the information sent on the MOSI line is data.
- 3. The serial data is available on MOSI and SPICLK clocks it into the register.
- 4. SS* goes high and D*/A goes high, indicating an end of communication. This action latches the Configuration Register bits.

When the SCXIbus is reset, all bits in the Configuration Register are cleared.

The Module ID Register connects to MISO on the SCXIbus. The Module ID Register is an 8-bit, parallel/serial-in, serial-out shift register and an SPI communication adapter. The contents of the Module ID Register are written onto MISO during the first four bytes of transfer after SS* has been asserted low. Zeros are written to MISO thereafter until SS* is released and reasserted. The SCXI-1120 module ID is hex 00000004.

Analog and Timing Circuitry

The SCXIbus provides analog power (± 18.5 VDC) that is regulated on the SCXI-1120 to ± 15 VDC, a guard, an analog bus (AB0 \pm), and a chassis ground (CHSGND). AB0 \pm buses the SCXI-1120 output to other modules or receives outputs from other modules via the SCXIbus. The guard guards the analog bus and can be connected via jumper W46 to the analog ground reference or can be left floating (a connection can be made by another board).

The data acquisition board analog input and timing is the interface between the SCXI-1120 output and the data acquisition board. This is described in the following section.

Analog Input Channels

Figure 3-5 is a diagram of the analog input block.



Figure 3-5. Analog Input Block Diagram

The analog input consists of eight isolated single-ended noninverting amplifiers. In addition, lowpass filtering is available at the inputs. You can jumper select one of two bandwidths, 10 kHz or 4 Hz. The amplifier gain is divided into two stages, a first stage providing gains of 1, 10, 50, and 100, and a second stage providing gains of 1, 2, 5, 10, and 20. Each channel is configurable to a different bandwidth and gain.

Use the following formula to determine the overall gain of a given amplifier input channel:

 $G_{total} = G_{1st} \times G_{2nd}$

where G_{total} is the overall gain and G_{1st} and G_{2nd} are the first- and second-stage gains. Here it is important to note that the choice of gain in each stage will affect the amplifier bandwidth. To determine the bandwidth of a given gain stage use the following formula:

BW = GBWP/G

where BW is a given amplifier stage bandwidth, GBWP is the gain bandwidth product (typically 800 kHz), and G is the gain at this stage. This BW might be of concern at high first-stage gains such as 50 and 100. In this case, the first-stage amplifier has a BW equal to 16 kHz and 8 kHz, respectively. Due to this decrease in the amplifier bandwidth, you will notice a decrease in the channel overall bandwidth, but a better noise immunity. If this bandwidth limitation is unacceptable, you should spread the gains over both stages, thus increasing the BW of each amplifier stage. This will introduce, in most cases, a negligible effect on the channel bandwidth. For example, to achieve a gain of 100, use $G_{1st} = 10$ and $G_{2nd} = 10$; for a gain of 1,000, use $G_{1st} = 50$ and $G_{2nd} = 20$.

All the amplifier input channels are overvoltage protected to 240 Vrms with power on or off.

The isolated amplifiers fulfill two purposes on the SCXI-1120 module. They convert a small signal riding on a high common-mode voltage into a single-ended signal with respect to the SCXI-1120 chassis ground. With this conversion, the input analog signal can be extracted from a high common-mode voltage or noise before being sampled and converted by the data acquisition board. The isolated amplifier also amplifies and conditions an input signal, which results in an increase in measurement resolution and accuracy.

After isolation, further filtering is available to increase the noise immunity of the amplifier channel. It is important to note that the overall amplifier bandwidth is determined by both filtering stages, so to achieve the required bandwidth, both filtering sections should be set the same, as indicated in Chapter 2, *Configuration and Installation*.

Calibration

Calibration Equipment Requirements

For best measurement results, calibrate the SCXI-1120 so that its offset is adjusted to $0 \pm 3 \text{ mV}$ RTO and $0 \pm 6 \mu \text{V}$ RTI. No special equipment is needed other than a regular voltmeter with the following specifications.

- Range: $\pm 30 \text{ mV}$ to $\pm 300 \text{ mV}$
- Resolution: 3 1/2 digits or greater

A multiranging 3 1/2-digit digital multimeter can provide you with the necessary function as described previously. We will refer to the measuring instrument as a digital multimeter (DMM).

Each channel on the SCXI-1120 has two potentiometers dedicated for calibration. One potentiometer is used to null the output offset; the other is used to null the input offset.

Offset Null Adjust

To null the offset of the amplifier channels, complete the following steps:

- 1. Set the DMM range to the smallest range that can measure ± 3 mV.
- 2. Short the inputs of the DMM together and then to chassis ground.
- 3. Record the measurement indicated by the DMM display. This is the DMM inherent offset and it should be subtracted from subsequent measurements.
- 4. Short the desired channel inputs together and then to chassis ground.
- 5. Set the amplifier gain to 1.
- 6. Connect the amplifier output to the DMM. Make sure that the DMM can achieve the accuracy and resolution you need.
- 7. Adjust the output potentiometer of the desired channel until the output is 0 ± 3 mV.
- 8. Set the DMM range to the smallest range that can measure ± 6 mV.
- 9. Set the amplifier gain to 1,000.
- 10. Adjust the input potentiometer of the desired channel until the output is 0 ± 6 mV.
- 11. Go to the next channel.

To avoid erroneous results when nulling the amplifier, follow these steps in the order indicated.

You may seal the potentiometers after calibration with antisabotage lacquer to avoid tampering with the calibration.

Table 3-2 lists the potentiometer reference designators that correspond to each channel.

Input Channel	Amplifier Channel	
Number	Input Null	Output
		Null
0	R8	R24
1	R10	R25
2	R12	R26
3	R14	R27
4	R16	R28
5	R18	R29
6	R20	R30
7	R21	R31

Table 3-2.	Calibration	Potentiometers	Reference	Designators
1 uoie 5 2.	Cumoration	1 otomioniotorio	renerence	Designators

Analog Output Circuitry

Figure 3-6 shows the SCXI-1120 analog output circuitry.



Figure 3-6. Analog Output Circuitry

The SCXI-1120 output circuitry consists of a buffered-output multiplexer and channel-select hardware. The channel-select hardware consists of a three-bit counter, MUXCOUNTER. This counter is needed when the board is operating in the Multiplexed-Output mode. The counter output is sent to the output multiplexer address pins to determine which of the eight channels is to be connected to MCH0. In the Single-Channel Read mode, the MUXCOUNTER is loaded with the desired channel number. In the Scanning mode, the counter is loaded with the first channel to be read. During the scan, the counter is clocked by SCANCLK from the data acquisition board, or TRIGO from the SCXIbus, depending on the state of the CLKSELECT bit in the Configuration Register. During scanning operations, the MUXCOUNTER is reloaded with the channel value stored in the Configuration Register when SCANCON is high (inactive), and will count upwards on each rising clock edge when SCANCON is low (active). In the Parallel-Output mode, the MUXCOUNTER is disabled and its output indicates binary 00; thus, amplifier Channel 0 is selected at the output multiplexer and is connected to MCH0. The seven other channels are hardwired to MCH1 through MCH7 on the rear signal connector.

The output multiplexer multiplexes all eight amplifier outputs and the temperature-sensor reading provided on the MTEMP line. To read the temperature sensor when it is multiplexed with the other input channels, the RTEMP bit of the Configuration Register must be set high. This measurement is only software controlled. For hardware control of the temperature sensor reading, connect the temperature sensor to pin 18 on the rear signal connector as described in Chapter 2, *Configuration and Installation*. The multiplexer output connects to the MCH0± and is connected to the data acquisition board analog channel input. In the case of the MIO data acquisition boards, MCH0± on the rear signal connector corresponds to ACH0 and ACH8.

Furthermore, the multiplexed output of the SCXI-1120 can be bused, via switches to $AB0\pm$ on the SCXIbus, to other modules. When you use multiple modules, it is possible to bus the module output via AB0 to the module that connects to the data acquisition board. In this case, the AB0 switches of all the modules are closed, whereas the output multiplexer of all the modules, except the one being read, are disabled. Refer to chapters 2 and 5 for further details on how to configure and program multiple modules.

In addition to the Multiplexed-Output mode described in the previous paragraph, it is possible to operate the SCXI-1120 in the Parallel-Output mode. In this mode, you need no software–other than the software used with your data acquisition board–to control the scanning of the eight channels or to perform a single read. To access the temperature sensor in this mode, configure the temperature sensor in the DTS mode. At power up or reset, amplifier Channel 0 is selected on the output multiplexer, and thus connects to MCH0. The other seven amplifier channels are hardwired to the rear signal connector. Notice that when the Multiplexed-Output mode is selected, pins 5 through 18 on the rear signal connector are still driven by the SCXI-1120. The SCXI-1120 outputs on the rear signal connector are short-circuit protected.

Refer to the following *Scanning Modes* section for further details on how to scan the SCXI-1120 channels.

Scanning Modes

The SCXI-1120 has four basic types of scanning modes–single-module parallel scanning, single-module multiplexed scanning, multiple-module multiplexed scanning, and multiple-chassis scanning, which is possible only with the SCXI-1001 chassis. For additional information, consult Chapter 2, *Configuration and Installation*, Chapter 5, *Programming*, your

data acquisition board user manual, or your SCXI chassis user manual. If you need more information, contact National Instruments.

Single-Module Parallel Scanning

Single-module parallel scanning is the simplest scanning mode. Directly cable the SCXI-1120 to the data acquisition board as shown in Figure 3-7. In this configuration, each analog signal has its own channel. Timing signals are not necessary for this type of scanning because the module provides all channels to the data acquisition board at all times. You can implement single-module parallel scanning with any data acquisition board that is appropriately cabled to the SCXI-1120.



Figure 3-7. Single-Module Parallel Scanning

Multiplexed Scanning

Only the MIO-16 data acquisition boards support multiplexed scanning on the SCXI-1120. During multiplexed scanning, a module sends the SCANCLK signal to Slot 0 over the TRIG0 backplane line, and Slot 0 sends SCANCON signals to each module. Each module uses its SCANCON signal to reload MUXCOUNTER and to determine when the SCXI-1120 output is enabled. Slot 0 contains a module scan list first-in-first-out (FIFO) memory chip, similar to the Channel/Gain FIFO on an MIO-16 board, except that instead of having a channel number and gain setting for each entry, the Slot 0 FIFO contains a slot number and a sample count for each entry. The list in Slot 0 will determine which module is being accessed and for how many samples. It is important that you make sure that the lists on the data acquisition board and Slot 0 are compatible so that the samples are acquired as intended. See your SCXI chassis manual for more information.

Single-Module Multiplexed Scanning

Single-Module Multiplexed Scanning (Direct)

This is the simplest multiplexed-scanning mode. Directly cable the SCXI-1120 to the data acquisition board as shown in Figure 3-8. The module sends SCANCLK onto TRIGO, and Slot 0 sends SCANCON back to the module. SCANCON will be low at all times during the scan

except during changes from one Slot 0 scan list entry to the next, when SCANCON pulses high to make the MUXCOUNTER reload its starting channel. Notice that although you are using only a single module, you can put many entries with different counts in the Slot 0 FIFO, so that some channels are read more often than others. You cannot change the start channel in the module Configuration Register during a scan.



Figure 3-8. Single-Module Multiplexed Scanning (Direct)

Single-Module Multiplexed Scanning (Indirect)

In this mode, the SCXI-1120 is not directly cabled to the data acquisition board. Instead, you connect another module to the data acquisition board, and the analog output of the SCXI-1120 is sent over Analog Bus 0, through the intermediate module, and then to the data acquisition board. The SCXI-1120 receives its MUXCOUNTER clock from TRIG0, which is sent by the intermediate module, as shown in Figure 3-9. Slot 0 operation is the same for direct connection scanning.



Figure 3-9. Single-Module Multiplexed Scanning (Indirect)

Multiple-Module Multiplexed Scanning

In this mode, all the modules tie into Analog Bus 0 and SCANCON enables the output of their amplifiers. The module that is directly cabled to the data acquisition board sends SCANCLK

onto TRIGO for the other modules and Slot 0, as shown in Figure 3-10. The scan list in Slot 0 is programmed with the sequence of modules and the number of samples per entry.



Figure 3-10. Multiple-Module Multiplexed Scanning

Multiple-Chassis Scanning

In this mode, you attach each SCXI-1001 chassis to a daisy chain of cable assemblies and multichassis adapter boards, as shown in Figure 3-11. You program each chassis separately, and each chassis occupies a dedicated channel of the data acquisition board. Within each chassis, scanning operations act as if the other chassis are not being used, with one exception—you must program the Slot 0 scan list in each chassis with dummy entries of Slot 13 to fill the samples when the data acquisition board will be sampling another chassis or data acquisition board channel. This will keep the chassis synchronized. Notice that you can only perform multiple-chassis scanning, for more information on multiple-chassis scanning. See Appendix E, *SCXI-1120 Cabling*, for more information on the necessary cable accessories for multichassis scanning.



Figure 3-11. Multiple-Chassis Scanning

Chapter 4 Register Descriptions

This chapter describes in detail the SCXI-1120 Module ID Register, the Configuration Register, the Slot 0 registers, and multiplexer addressing.

Note: If you plan to use a programming software package such as NI-DAQ, LabWindows, or LabVIEW with your SCXI-1120 board, you do not need to read this chapter.

Register Description

Register Description Format

This register description chapter discusses each of the SCXI-1120 registers and the Slot 0 registers. A detailed bit description of each register is given. The individual register description gives the type, word size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB shown on the left (bit 15 for a 16-bit register, bit 7 for an 8-bit register), and the LSB shown on the right (bit 0). A rectangle is used to represent each bit. Each bit is labeled with a name inside its rectangle. An asterisk (*) after the bit name indicates that the bit is inverted (negative logic). The Module ID register has a unique format and is described in the *Module ID Register* section.

In many of the registers, several bits are labeled with an X, indicating don't care bits. When you write to a register, you may set or clear these bits without effect.

SCXI-1120 Registers

The SCXI-1120 has two registers. The Module ID Register is a four-byte, read-only register that contains the Module ID number of the SCXI-1120. The Configuration Register is a 16-bit, write-only register that controls the functions and characteristics of the SCXI-1120.

Module ID Register

The Module ID Register contains the 4-byte module ID code for the SCXI-1120. This code number will be read as the first four bytes on the MISO line whenever the module is accessed. The bytes will appear least significant byte first. Within each byte, data is sent out MSB first. Additional data transfers will result in all zeros being sent on the MISO line. The Module ID Register is reinitialized to its original value each time the SCXI-1120 is deselected by the SS* signal on the backplane.

Type:	Read-on	ly					
Word Size:	4-byte						
Bit Map:							
Byte 0							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
Byte 1 7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Byte 2	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Byte 3	6	5	4	3	2	1	0
1 0	0	1 0	I U	1 0	1 0	1 0	0

Configuration Register

The Configuration Register contains 16 bits that control the functions of the SCXI-1120. When SS^* is asserted (low) and D^*/A indicates data (low), the register will shift in the data present on the MOSI line, bit 15 first, and then latch it when the SCXI-1120 is deselected by the SS* signal on the backplane. The Configuration Register initializes to all zeros when the SCXI chassis is reset or first turned on.

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
CLKOUTEN	CLKSELECT	Х	Х	Х	CHAN2	CHAN1	CHAN0
7	6	5	4	3	2	1	0
Х	Х	RTEMP	RSVD	SCANCLKEN	SCANCONEN	AB0EN	FOUTEN*

Bit	Name	Description				
15	CLKOUTEN	Scan Clock Output Enable – This bit determines whether the SCANCLK signal from the rear signal connector is sent out, in inverted form, to the TRIGO backplane signal. If CLKOUTEN is set to 1, SCANCLK* is transmitted on TRIGO. If CLKOUTEN is cleared to 0, SCANCLK* is not transmitted on TRIGO.				
14	CLKSELECT	Scan Clock Select – This bit determines whether the SCXI-1120 uses SCANCLK or the inverted form of TRIG0 to clock the MUXCOUNTER for the purposes of scanning through the analog channels. If CLKSELECT is cleared to 0, SCANCLK is used to clock MUXCOUNTER. If CLKSELECT is set to 1, TRIG0* is used as the source to clock MUXCOUNTER.				
13-11, 7-6	Х	Don't care bits – Unused.				
10-8	CHAN<20>	Channel Select – These bits determine the channel number (zero to seven) that is loaded into the MUXCOUNTER to determine the analog channel to be read during a single read, or the starting channel on the module for a scanned data acquisition. CHAN2 is the MSB.				

Bit	Name	Description (continued)
5	RTEMP	Read Temperature – This bit determines whether the selected channel output or the MTEMP signal is driven onto the MCH0± pins of the rear signal connector. If RTEMP is cleared to 0, the selected channel output is used as the module output. If RTEMP is set to 1, the MTEMP signal is used as the module output. The module output will only be driven when FOUTEN* is cleared to 0, or SCANCON is active (low) while SCANCONEN* is cleared.
4	RSVD	Reserved – This bit should always be written to 0.
3	SCANCLKEN	Scan Clock Enable – This bit determines whether MUXCOUNTER will increment on each clock signal (the clock source is determined by CLKSELECT), or keep its loaded value. If SCANCLKEN is set to 1, MUXCOUNTER will be clocked during scans. If SCANCLKEN is cleared to 0, MUXCOUNTER will not be clocked.
2	SCANCONEN	Scan Control Enable – This bit, when set to 1, enables the SCANCON signal.
1	AB0EN	Analog Bus 0 Enable – This bit determines whether Analog Bus 0 on the SCXIbus drives MCH0 on the rear signal connector. If AB0EN is cleared to 0, Analog Bus 0 doesnot drive MCH0. If AB0EN is set to 1, Analog Bus 0 + drives MCH0+ through a buffer and a Analog Bus 0 - is connected to MCH0
0	FOUTEN*	Forced Output Enable – This bit determines whether the module will drive the MCH0± pins on the rear signal connector with either the selected channel output or the MTEMP signal, depending on the state of RTEMP. If FOUTEN* is cleared to 0, the MCH0± pins will be driven through a buffer by the selected channel output or the MTEMP line. If FOUTEN* is set to 1, the MCH0± pins will not be driven by the selected channel output or MTEMP, unless SCANCON is active (low) and the SCANCONEN bit is cleared. If the selected channel output or MTEMP is driving the output buffer, it will drive Analog Bus 0 if AB0EN is set. If nothing is driving the output buffer, the SCXI-1120 output will saturate.

Slot 0 Register Descriptions

Slot 0 has three registers. The Slot-Select Register is a 16-bit, write-only register that determines with which slot the data acquisition board will speak when SLOT0SEL* is released high. In the case of the SCXI-1001 chassis, the Slot-Select Register also determines in which chassis the desired slot is. The FIFO Register is a 16-bit, write-only register used for storing the Slot 0 scan list that determines the chassis scan sequence. The Hardscan Control Register (HSCR) is an 8-bit, write-only register used for setting up the timing circuitry in Slot 0. The Slot-Select Register is written to by using the SLOT0SEL* line. The HSCR and the FIFO Register are written to as if they were registers located on modules in Slots 13 and 14. You should maintain software copies of the Slot-Select Register, HSCRs, and all the Slot 0 scan lists that correspond to the writes to FIFO Registers.

If you are using multiple chassis, it is important to understand the architectural differences of the Slot-Select Register as compared to the HSCR and the FIFO Register. Although each chassis has its own physical Slot-Select Register, all are written to at the same time. The jumper settings in Slot 0 of a chassis determine with which chassis number Slot 0 is identified. From the software perspective, only one Slot-Select Register exists in a system composed of multiple chassis. The HSCR and FIFO Register, on the other hand, are unique to each chassis and you must program them separately.

Slot-Select Register

Write-only

Type:

The Slot-Select Register contains 16 bits that determine which module in which chassis will be enabled for communication when the SLOTOSEL* line is high. An SCXI-1000 chassis will select the appropriate module in its chassis, regardless of the chassis number written. The Slot-Select Register will shift in the data present on the MOSI line, bit 16 first, when SLOTOSEL* is low.

Word Size:	16-bit						
Bit Map:							
1.5	1.4	10	10	11	10	0	0
15	14 	13	12 V	II v	10 V	9 V	8
X	X	X	X	X	X	X	CHS4
7	6	5	4	3	2	1	0
CHS3	CHS2	CHS1	CHS0	SL3	SL2	SL1	SL0
Bit	Name		Descriptio	on			
15-9	Х		Don't care	bits – Unus	1098XXCHS4210SL2SL1SL0		
8-4	CHS<4.	.0>	Chassis Bi which cha chassis, th	Chassis Bit 4 through 0 – These bits determine which chassis is selected. On the SCXI-1000 chassis, these are don't care bits.			
3-0	SL<30	>	Slot Bit 3 slot in the	through 0 – selected cha	These bits de	etermine wh	ich

Hardscan Control Register (HSCR)

The HSCR contains eight bits that control the setup and operation of the hardscan timing circuitry of Slot 0. To write to the HSCR, follow the procedure given in the *Register Writes* section in Chapter 5, *Programming*, using 13 as the slot number and writing eight bits to the HSCR. The register will shift in the data present on the MOSI line, bit 7 first, when Slot 13 is selected by the Slot-Select Register.

Type:	Write-only
V 1	-

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
RSVD	FRT	RD	ONCE	HSRS*	LOAD*	SCANCONEN	CLKEN
Bit	Name		Descripti	on			
7	RSVD		Reserved.				
6	FRT		Forced Re list in the allowing t instead of set, it has	etransmit – T FIFO to be r the scan list t having to re no effect.	This bit, whe einitialized to be reprog write the en	en clear, cause to the first en rammed in tw tire list. Whe	es the scan atry, thus vo steps en this bit is
5	RD		Read – Th read. Wh of a scan disabled t	his bit, when en set, the Fl list entry dur o advance to	clear, preve IFO is being ing scannin the next sc	ents the FIFO g read except g, when readi an list entry.	from being at the end ng is briefly
4	ONCE		Once – When set, this bit will cause the Hardscan circuitry to shut down at the end of the scan list circuitry during a data acquisition. When clear, the circuitry will wrap around and continue seamlessly with the first scan list entry after the entry is finished.				
3	HSRS*		Hardscan hardware to the pov	Reset – Whe scanning circ ver up state.	en clear, this cuitry, inclu When set, t	s bit causes al ding the FIF(his bit has no	l the D, to be reset effect.
2	LOAD*		Load – T sample co this bit ha	his bit, when ounter with th s no effect.	clear, force ne output of	es a loading o the FIFO. W	f the Slot 0 ⁷ hen set,
1	SCANCO	NEN	Scan Con SCANCC disabled (trol Enable – N lines. Wh high).	When set, hen clear, al	this bit enable l SCANCON	es the lines are
0	CLKEN		Clock Ena clock for disabled.	able – When the hardscan	set, this bit circuitry. V	enables TRIC When clear, T	30 as a ƁIG0 is

FIFO Register

The FIFO Register is used to add entries to the Slot 0 FIFO. The FIFO contains the Slot 0 scan list. Each entry contains a slot number to be accessed, and a count number to determine the number of samples to be taken from that slot. To write to the FIFO Register, follow the procedure given in the *Register Writes* section in Chapter 5, *Programming*, using 14 as the slot number, and writing 16 bits to the FIFO Register. The register will shift in the data present on the MOSI line, bit 7 first, when Slot 14 is selected by the Slot-Select Register. The Slot 0 scan list is created by consecutive writes to the FIFO Register. Each write creates a new entry at the end of the scan list. The maximum number of entries is 256. To clear the FIFO of all entries, clear the HSRS* bit in the HSCR.

Type: Write-only

Word Size: 16-bit

Bit Map:

15	14	13	12	11	10	9	8
X	Х	Х	Х	X	MOD3	MOD2	MOD1
7	6	5	4	3	2	1	0
MOD0	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
Bit	Ν	Name	De	escription			
15-11	Σ	K	Do	Don't care bits – Unused.			
10-7	Ν	MOD<30>	Me de thi Me	Module Number – The value of these bits plus determines the number of the slot to be accesse this scan entry. For example, to access Slot 6, MOD<30> would be 0101.			
6-0	C	CNT<60>	Co ho sca co co	ount – The v w many sam an list entry l rresponds to rresponds to	alue of these ples will be becomes action one sample 128 samples	e bits plus or taken before ive. A value and a value s.	ne determines e the next e of zero of 127

Chapter 5 Programming

This chapter contains a functional programming description of the SCXI-1120 and Slot 0.

Note: If you plan to use a programming software package such as NI-DAQ, LabWindows, or LabVIEW with your SCXI-1120 board, you do not need to read this chapter.

Programming Considerations

Programming the SCXI-1120 involves writing to the Configuration Register. Programming Slot 0 involves writing to the HSCR and FIFO Register. Programming the data acquisition boards involves writes to their registers. See your data acquisition board user manual for more information. The programming instructions list the sequence of steps to take. The instructions are language independent; that is, they instruct you to write a value to a given register without presenting the actual code.

Notation

For the bit patterns to be written, the following symbols are used:

- 0 binary zero
- 1 binary one
- X don't care; either zero or one may be written
- C one of three bits used to specify the channel to be loaded into the MUXCOUNTER. This value will either be the channel to be read for single reads, or a starting channel for scanned measurements.

The 16-bit patterns are presented MSB first, left to right.

Register Writes

This section describes how to write to the Configuration Register, HSCR, and FIFO Register, including the procedure for writing to the Slot-Select Register to select the appropriate slot. For timing specifics, refer to the *Timing Requirements and Communication Protocol* section in Chapter 2, *Configuration and Installation*. The rear signal connector pin equivalences to the different National Instruments data acquisition boards are given in Table 5-1. Also see Appendix E, *SCXI-1120 Cabling*. The Configuration Register, the HSCR, and the FIFO Register are write-only registers.

The different bits in these registers often control independent pieces of circuitry. There are times when you may want to set or clear a specific bit or bits without affecting the remaining bits. However, a write to one of these registers will affect all bits simultaneously. You cannot read the registers to determine which bits have been set or cleared in the past; therefore, you should maintain a software copy of these registers. You can then read the software copy to determine the status of the register. To change the state of a single bit without disturbing the remaining bits, set or clear the bit in the software copy and write the software copy to the register.
SCXIbus Line	SCXI-1120 Rear Signal Connector	MIO-16 Board	Lab-NB/Lab-PC/ Lab-PC+/Lab-LC	PC-LPM-16
MOSI	SERDATIN	ADIO0	PB4	DOUT4
D*/A	DAQD*/A	ADIO1	PB5	DOUT5
INTR*	SLOT0SEL*	ADIO2	PB6	DOUT6
SPICLK	SERCLK	EXTSTROBE*	PB7	DOUT7
MISO	SERDATOUT	BDIO0	PC1	DIN6

Table 5-1.	SCXI-1120	Rear Signal	Connector I	Pin Equivalences
10010 0 11	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		0011100001	

Register Selection and Write Procedure

1. Select the slot of the module to be written to (or Slot 13 or 14). Initial conditions:

SERDATIN = X. DAQD*/A = X. SLOT0SEL* = 1. SERCLK = 1.

- 2. Clear SLOT0SEL* to 0. This will deassert all SS* lines to all modules in all chassis.
- 3. For each bit, starting with the MSB (bit 15):
 - a. SERDATIN = bit to be sent. These bits are the data that is being written to the Slot-Select Register.
 - b. Clear SERCLK to 0.
 - c. Set SERCLK to 1. This rising edge clocks the data. (If you are using an MIO-16 board, writing to the EXTSTROBE* register will pulse EXTSTROBE* low and then high, accomplishing steps 3b and 3c.)
- 4. Set SLOT0SEL* to 1. This will assert the SS* line of the module whose slot number was written to Slot 0. If you are using multiple chassis, only the appropriate slot in the chassis whose address corresponds to the written chassis number will be selected automatically. When no communications are taking place between the data acquisition board and any modules, write zero to the Slot-Select Register to ensure that no accidental writes occur.
- 5. If you are writing to a Configuration Register, clear DAQD*/A to 0 (this indicates data will be written to Configuration Register). If you are writing to the HSCR or FIFO Register, leave DAQD*/A high.
- 6. For each bit to be written to the Configuration Register:
 - a. Establish desired SERDATIN level corresponding to this bit.
 - b. Clear SERCLK to 0.
 - c. Set SERCLK to 1 (clock the data). (If you are using an MIO-16 board, writing to the EXTSTROBE* register will pulse EXTSTROBE* low and then high, accomplishing steps 6b and 6c.)

- 7. Pull SLOT0SEL* low to deassert the SS* line, latch the data into the Configuration Register and establish conditions for writing a new slot-select number to the Slot 0 Slot-Select Register.
- 8. If you are not selecting another slot, write zero to the Slot 0 Slot-Select Register. If you are selecting another slot, start at step 3.

For a timing illustration of a Configuration Register write, see Figure 2-15, *Configuration Register Write Timing Diagram*, which shows the proper write to configure an SCXI-1120 that is directly cabled to an MIO-16 board for multiple-module multiplexed scanning with a start channel of 3.

Initialization

The SCXI-1120 powers up with its Configuration register cleared to all zeros. You can force this state by sending an active low signal on the RESET* pin of the SCXIbus connector. In the reset state, CH0 through CH3 are routed to MCH0 through MCH3 on the rear signal connector. The module is disconnected from Analog Bus 0 and disabled from scanning.

Single-Channel Measurements

This section describes how to program the SCXI-1120, either alone or in conjunction with other modules, to make single-channel, or nonscanned, measurements.

Direct Measurements

Parallel Output

To perform a parallel output measurement, you must cable the SCXI-1120 rear signal connector to a data acquisition board with each output connected to a different data acquisition board channel. See Chapter 2, *Configuration and Installation*, for more information. For information on how to make the voltage measurement with your data acquisition board, consult your data acquisition board user manual. Remember to account for the gains of both the SCXI-1120 and the data acquisition board when calculating the actual voltage present at the input of the SCXI-1120.

To measure one of the eight differential input channels to the SCXI-1120, or the DTEMP line if the module has been configured appropriately, perform the following steps:

- 1. Write the binary pattern 00XXX000 XX000000 to the SCXI-1120 Configuration Register. Notice that this can be the RESET state.
- 2. Measure the voltage with the data acquisition board.

Multiplexed Output

To perform a direct multiplexed output measurement, you must cable the SCXI-1120 rear signal connector to a data acquisition board. See Chapter 2, *Configuration and Installation*, for more information. For information on how to make the voltage measurement with your data acquisition board, consult your data acquisition board user manual. Remember to account for the gains of both the SCXI-1120 and the data acquisition board when calculating the actual voltage present at the input of the SCXI-1120.

To measure one of the eight differential input channels to the SCXI-1120, perform the following steps:

- 1. Write the binary pattern 00XXXXCC XX000000 to the SCXI-1120 Configuration Register.
- 2. Measure the voltage with the data acquisition board.

To measure the voltage on the MTEMP line, perform the following steps:

- 1. Write the binary pattern 00xxxxxx xx100000 to the SCXI-1120 Configuration Register.
- 2. Measure the voltage with the data acquisition board.

Indirect Measurements

Indirect measurements involve one module sending a signal to Analog Bus 0, where it is picked up by another module and transmitted to the data acquisition board.

Measurements from Other Modules

To perform measurements from other modules, you must cable the SCXI-1120 rear signal connector to a data acquisition board. See Chapter 2, *Configuration and Installation*, for more information. To make a measurement from another module, perform the following steps:

- 1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1120, clearing AB0EN in the Configuration Register will ensure that its output is not driving AB0.
- 2. Write the binary pattern 00XXXXXX XX100011 to the SCXI-1120 Configuration Register. This step disables the SCXI-1120 from driving Analog Bus 0 and allows Analog Bus 0 to drive MCH0 through the output buffer.
- 3. Program the other module to drive Analog Bus 0 with the signal to be measured.
- 4. Measure the voltage with the data acquisition board.

Measurements from the SCXI-1120 via Another Module

To perform measurements via another module, you must cable the other module rear signal connector to a data acquisition board. The other module must be able to transfer Analog Bus 0 to the data acquisition board. See Chapter 2, *Configuration and Installation*, for more information.

To measure one of the eight differential input channels to the SCXI-1120, perform the following steps:

- 1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1120, clearing AB0EN in the Configuration Register will ensure that its output is not driving AB0.
- 2. Program the other module not to drive Analog Bus 0, but to send Analog Bus 0 to the data acquisition board.
- 3. Write the binary pattern 00XXXCCC XX000010 to the SCXI-1120 Configuration Register.
- 4. Measure the voltage with the data acquisition board.

To measure the voltage on the MTEMP line, perform the following steps:

- 1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1120, clearing AB0EN in the Configuration Register will ensure that its output is not driving AB0.
- 2. Program the other module not to drive Analog Bus 0, but to send Analog Bus 0 to the data acquisition board.
- 3. Write the binary pattern 00xxxxxx xx100010 to the SCXI-1120 Configuration Register.
- 4. Measure the voltage with the data acquisition board.

Scanning Measurements

Programming for scanned data acquisition involves programming your data acquisition board, modules, and Slot 0. In general, the steps to be taken are as follows:

- 1. Perform all data acquisition board programming to the point of enabling the data acquisition.
- 2. Perform all module programming.
- 3. Program the Slot 0 hardscan circuitry.
- 4. Enable the data acquisition, trigger it either through software or hardware, and service the data acquisition.

The MIO boards can do all types of scanning. Lab-NB, Lab-PC, Lab-PC+, Lab-LC, and PC-LPM-16 boards support only single-module parallel scanning, and do not support any of the multiplexed scanning modes. Notice that single-module parallel scanning is typically done without any module or Slot 0 programming; only programming the data acquisition board is necessary.

1. Data Acquisition Board Setup Programming

The programming steps for your data acquisition board are given in your data acquisition board user manual. You should follow the instructions in the following sections:

- AT-MIO-16 User Manual
 - Multiple A/D Conversions with Continuous Channel Scanning (Round Robin)
 - Multiple A/D Conversions with Interval Channel Scanning (Pseudosimultaneous)
- AT-MIO-16D User Manual
 - Multiple A/D Conversions with Continuous Channel Scanning (Round Robin)
 - Multiple A/D Conversions with Interval Channel Scanning (Pseudosimultaneous)
- AT-MIO-16F-5 User Manual
 - Posttrigger Data Acquisition with Continuous Channel Scanning
 - Posttrigger Data Acquisition with Interval Channel Scanning
- AT-MIO-16X User Manual
 - Continuous Channel Scanning Data Acquisition
 - Interval Channel Scanning Data Acquisition
- AT-MIO-64F-5 User Manual
 - Continuous Channel Scanning Data Acquisition
 - Interval Channel Scanning Data Acquisition
- Lab-LC User Manual
 - Programming Multiple A/D Conversions with Channel Scanning
- Lab-NB User Manual
 - Programming Multiple A/D Conversions with Channel Scanning
- Lab-PC User Manual
 - Programming Multiple A/D Conversions with Channel Scanning
- Lab-PC+ User Manual
 - Programming Multiple A/D Conversions with Channel Scanning
 - Programming Multiple A/D Conversions with Interval Scanning
 - Programming Multiple A/D Conversions in Single-Channel Interval Acquisition Mode

- MC-MIO-16 User Manual
 - Multiple A/D Conversions with Continuous Channel Scanning (Round Robin)
 - Multiple A/D Conversions with Interval Channel Scanning (Pseudosimultaneous)
- NB-MIO-16 User Manual
 - Programming Multiple A/D Conversions with Channel Scanning
- NB-MIO-16X User Manual
 - Multiple A/D Conversions with Continuous Channel Scanning (Round Robin)
 - *Multiple A/D Conversions with Interval Channel Scanning (Pseudosimultaneous)*
- PC-LPM-16 User Manual
 - Programming Multiple A/D Conversions with Channel Scanning

Follow the instructions in these sections through the part labeled as follows:

- *Clear the A/D Circuitry and Reset the Mux Counter* in the MIO board user manual (except for the AT-MIO-16X and AT-MIO-64F-5). Do not continue to the part called *Enable the Scanning Data Acquisition Operation*. You will do this after you have programmed the modules and Slot 0.
- *Program the Sample Counter* (if you are doing continuous channel scanning) or *Program the Scan-Interval Counter* (if you are doing interval channel scanning) in the AT-MIO-16X and AT-MIO-64F-5 user manuals. Do not continue to the part labeled *Enable a Scanning Data Acquisition Operation* or *Enable an Interval Scanning Data Acquisition Operation*. You will do this after you have programmed the modules and Slot 0.
- **Note:** For multiplexed scanning with an MIO board, it is important that you follow the instructions in the channel scanning sections, not the single-channel sections. Although you may be using only one MIO board channel, the channel scanning programming will ensure that the MIO board outputs SCANCLK, which is needed by the SCXI-1120 and Slot 0.
- *Clear the A/D Circuitry* in the *Lab-LC User Manual*. Do not continue to the part called *Program the Sample-Interval Counter*. You will do this after you have programmed the modules and Slot 0.
- *Clear the A/D Circuitry* in the *Lab-PC User Manual*, the *Lab PC+ User Manual*, and the *PC-LPM-16 User Manual*. Do not continue to the part called *Start and Service the Data Acquisition Operation*. You will do this after you have programmed the modules and Slot 0.
- *Clear the A/D Circuitry* in the *Lab-NB User Manual*. Do not continue to the part called *Program the Sample-Interval Counter (Counter A0)*. You will do this after you have programmed the modules and Slot 0.

Counter 1 and SCANDIV

All MIO boards can operate their data acquisition board scan lists in two ways—they can acquire one sample per data acquisition board scan list entry; or they can acquire N samples per data acquisition board scan list entry, where N is a number from 2 to 65,535 that is programmed in Counter 1. This second method of operation is especially useful when the data acquisition board scan list length is limited to 16 entries, as it is on all MIO boards except the AT-MIO-16F-5, which can have up to 512 entries. Because you can multiplex many SCXI-1120s in one chassis to one MIO board channel, often the simplest way to program the MIO board is to use only one data acquisition board scan list entry, and make N the total number of samples to be taken on all modules in one scan. Check your MIO board user manual for limitations in the data acquisition board scan list format.

To program the MIO board to take *N* samples per data acquisition board scan list entry, perform the following additional programming steps at the end of the *Enable the Scanning Data Acquisition Operation* section in the appropriate data acquisition board user manual:

- 1. Write FF01 to the Am9513 Command Register to select Counter 1 Mode Register.
- 2. Write 0325 (hex) to the Am9513 Data Register to store Counter 1 Mode Value for most MIO boards. For the AT-MIO-16F-5, and the AT-MIO-16X, and the AT-MIO-64F-5, write 1325 (hex).
- 3. Write FF09 to the Am9513 Command Register to select Counter 1 Load Register.
- 4. Write the number of samples to be taken per scan list entry (2 to 65,535) to the Am9513 Data Register to load Counter 1.
- 5. Write FF41 to the Am9513 Command Register to load Counter 1.
- 6. Write FFF1 to the Am9513 Command Register to step Counter 1.
- 7. Write FF21 to the Am9513 Command Register to arm Counter 1.
- 8. Set the SCANDIV bit in Command Register 1.

2. Module Programming

This section describes the programming steps for various scanning possibilities.

Single-Module Parallel Scanning

To perform single-module parallel scanning, you must cable the SCXI-1120 rear signal connector to a data acquisition board with each output connected to a different data acquisition board channel. See Chapter 2, *Configuration and Installation*, for more information.

To program the SCXI-1120 for single-module parallel scanning, write the binary pattern 00xxxx00 xx000000 to the SCXI-1120 Configuration Register. Notice that this can be the RESET state.

Single-Module Multiplexed Scanning (Direct)

To perform simple channel scanning, you must cable the SCXI-1120 to a data acquisition board. See Chapter 2, *Configuration and Installation*, for more information.

To program the module for scanned-channel measurements, write the binary pattern 10XXXCCC XX001101 to the SCXI-1120 Configuration Register. CCC represents the starting channel number.

Single-Module Multiplexed Scanning (Indirect)

To indirectly scan a module, send the output of the scanned module onto Analog Bus 0, where it is picked up by another module and transmitted to the data acquisition board.

<u>Channel Scanning from Other Modules.</u> To scan measurements from other modules, you must cable the SCXI-1120 to a data acquisition board. See Chapter 2, *Configuration and Installation*, for more information. The module programming steps are as follows:

- 1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1120, clearing AB0EN in the Configuration Register will ensure that its output is not driving AB0.
- 2. Write the binary pattern 10XXXXXX XX100011 to the SCXI-1120 Configuration Register. This step disables the SCXI-1120 from driving Analog Bus 0 and allows Analog Bus 0 to drive MCH0 through the output buffer.
- 3. Program the other module to be scanned.

<u>Channel Scanning from the SCXI-1120 via Another Module.</u> To scan the SCXI-1120 via other modules, you must cable the other module to a data acquisition board, and the other module must be able to transfer Analog Bus 0 to the data acquisition board. The other module must also be able to send a SCANCLK*-compatible signal on TRIG0. See Chapter 2, *Configuration and Installation*, for more information. The module programming steps are as follows:

- 1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1120, clearing AB0EN in the Configuration Register will ensure that its output is not driving AB0.
- 2. Program the other module not to drive Analog Bus 0, but to send Analog Bus 0 to the data acquisition board. Also program the other module to send a SCANCLK*-compatible signal to TRIG0.
- 3. Write the binary pattern 01XXXCCC XX001111 to the SCXI-1120 Configuration Register, where CCC is the starting channel number.

Multiple-Module Multiplexed Scanning

To scan multiple modules, you must connect one module to the data acquisition board, and the module must be able to transfer Analog Bus 0 to the data acquisition board. This module must

also be able to send a SCANCLK*-compatible signal on TRIG0. See Chapter 2, *Configuration and Installation*, for more information. The module programming steps are as follows:

- 1. Perform any necessary programming to ensure that no modules are driving Analog Bus 0. For an SCXI-1120, clearing AB0EN in the Configuration Register will ensure that its output is not driving AB0.
- 2. Program the module that is connected to the data acquisition board to connect Analog Bus 0 to the data acquisition board but not drive Analog Bus 0 unless it is receiving an active low signal on SCANCON. Also program the module to send a SCANCLK*-compatible signal onto TRIG0. If this module is an SCXI-1120, this programming is accomplished by writing the binary pattern 10XXXCCC XX001111 to its Configuration Register.
 - **Note:** If this module is an SCXI-1120 and is not going to be scanned (it is just being used as an interface), write a 0 to bit 2 (SCANCONEN) in the Configuration Register. The start channel bits become don't care bits.
- 3. Program the other modules to be used in the scan to connect their outputs to Analog Bus 0 but not drive Analog Bus 0 unless receiving an active low signal on SCANCON. Also program the modules to use TRIGO as their clock source. For SCXI-1120 modules, this programming is accomplished by writing the binary pattern 01XXXCCC XX001111 to their Configuration Registers.

Multiple-Chassis Scanning

To scan modules on multiple chassis, you must use the SCXI-1001 chassis. The cable from the data acquisition board must bus the digital lines to one module on each chassis. Additionally, the cable must provide each chassis with its own analog channel. The data acquisition board must be able to take several readings at a time on a given channel before accessing a new channel. See the *Counter 1 and SCANDIV* subsection of the *1. Data Acquisition Board Setup Programming* section earlier in this chapter. You can use the MIO-16 boards, in conjunction with the SCXI-1350 multichassis adapter, for multichassis scanning.

For each chassis, program the modules according to the appropriate mode of operation, disregarding the fact that other chassis will be involved.

For example, you want to scan thirteen modules. Twelve modules are in one chassis, and the thirteenth is in the second chassis and is to be scanned through a fourteenth module that is cabled to the data acquisition board but is not involved in the scan. Program the twelve modules in the first chassis according to the steps in the previous *Multiple-Module Multiplexed Scanning* section, and program the thirteenth and fourteenth modules according to *Channel Scanning from the SCXI-1120 via Another Module* earlier in this chapter.

3. Programming the Slot 0 Hardscan Circuitry

The following section describes how to program the Slot 0 circuitry for scanning operations. For a more detailed description of the Slot 0 scanning circuitry, consult the *SCXI-1000/1001 User Manual*. Descriptions of the Slot 0 registers are in the *Slot 0 Register Descriptions* section of Chapter 4, *Register Descriptions*. It is not necessary to read this section if you are performing single-module parallel scanning.

To program the hardscan circuitry, perform the following steps:

- 1. Write binary 0000 0000 to the HSCR.
- 2. Write binary 0000 1000 to the HSCR.
- 3. Write the Slot 0 scan list to the FIFO.
- 4. Write binary 0010 1100 to the HSCR.
- 5. Write binary 101S 1100 to the HSCR.
- 6. Write binary 101S 1110 to the HSCR.
- 7. Write binary 101S 1111 to the HSCR.

To program the hardscan circuitry to use the current scan list, perform the following steps:

- 1. Write binary 0000 1000 to the HSCR.
- 2. Write binary 0100 1000 to the HSCR.
- 3. Write binary 0000 1000 to the HSCR.
- 4. Write binary 0010 1100 to the HSCR.
- 5. Write binary 101S 1100 to the HSCR.
- 6. Write binary 101S 1110 to the HSCR.
- 7. Write binary 101S 1111 to the HSCR.

In the preceding steps:

- S = 0 if you want the scanning to repeat when the end of the list is reached.
- S = 1 if you want the circuitry to shut down after a single scan.

When you are writing multiple entries to the same register, for example, repetitive writes to the HSCR or several FIFO entries, it is important that SS*13 or SS*14 go inactive (high) between each entry. Select another slot or toggle the SLOTOSEL* line to temporarily deassert the appropriate SS* line.

If consecutive scan list entries access an SCXI-1120, the module will reload the MUXCOUNTER with the starting channel after each entry. Thus, two entries with counts of four for one module will yield different behavior than one entry with a count of eight.

For multiple-chassis scanning, program each Slot 0 with dummy entries to fill the sample counts when the data acquisition board is accessing other chassis. Use Slot 13 as the dummy entry slot.

See *Example 3* at the end of this chapter.

4. Acquisition Enable, Triggering, and Servicing

At this point, you should now continue from where you left off in the *1*. *Data Acquisition Board Setup Programming* section of this chapter. Perform the following steps given in your data acquisition board user manual.

- MIO board user manual
 - Enable the scanning data acquisition operation.
 - Apply a trigger.
 - Service the data acquisition operation.
- Lab-PC User Manual, Lab-PC+ User Manual, and PC-LPM-16 User Manual
 - Start and service the data acquisition operation.
- Lab-LC User Manual
 - Program the sample-interval counter.
 - Service the data acquisition operation.
- Lab-NB User Manual
 - Program the sample-interval counter (Counter A0).
 - Service the data acquisition operation.

Scanning Examples

The following examples are intended to aid your understanding of module and Slot 0 programming. It will be helpful to refer to the bit descriptions for the Configuration Register and the FIFO Register in Chapter 4, *Register Descriptions*.

Example 1

You want to scan, in Multiplexed mode, channels 1 through 4 on an SCXI-1120 in Slot 1 of an SCXI-1000 chassis. The SCXI-1120 is directly cabled to a data acquisition board.

The programming steps are as follows:

- 1. Program your data acquisition board as described in the *1. Data Acquisition Board Setup Programming* section of this chapter.
- 2. Following the procedure given in the *Register Writes* section, write 10000100 00001101 to the Configuration Register of the SCXI-1120 in Slot 1.

3. Follow the steps outlined in the section earlier in this chapter, *3. Programming the Slot 0 Hardscan Circuitry*, where step 3, *Write the Slot 0 scan list to the FIFO*, consists of the following:

Write 0000000 0000011 to the FIFO Register. This corresponds to Slot 1 for four samples.

4. Follow the procedure given in the 4. Acquisition Enable, Triggering, and Servicing section earlier in this chapter.

Example 2

An SCXI-1000 chassis has four SCXI-1120 modules in Slots 1, 2, 3, and 4. The SCXI-1120 in Slot 4 is cabled to the data acquisition board. You want to scan channels 3 through 7 on the SCXI-1120 in Slot 1, channels 0 through 6 on the SCXI-1120 in Slot 4, and channels 7 through 3 on the SCXI-1120 in Slot 3.

The programming steps are as follows:

- 1. Program your data acquisition board as described in the *1. Data Acquisition Board Setup Programming* section.
- 2. Following the procedure given in the *Register Writes* section, write 00000000 00000000 to the Configuration Register of the SCXI-1120 in Slot 2. This step resets the module, including the clearing of the AB0EN bit (bit 0). Notice that a complete reset of this module is not necessary, but is used for simplicity.
- 3. Following the procedure given in the *Register Writes* section, write 10XXX000 00001111 to the Configuration Register of the SCXI-1120 in Slot 4.
- 4. Following the procedure given in the *Register Writes* section, write 01XXX011 00001111 to the Configuration Register of the SCXI-1120 in Slot 1.
- 5. Following the procedure given in the *Register Writes* section, write 01XXX111 00001111 to the Configuration Register of the SCXI-1120 in Slot 3. Notice that after Channel 7, the SCXI-1120 will *wrap around* to Channel 0.
- 6. Follow the steps given in the section earlier in this chapter, 3. *Programming the Slot 0 Hardscan Circuitry*, where step 3, *Write the Slot 0 scan list to the FIFO*, consists of the following:
 - a. Write 00000000 00000100 to the FIFO Register. This corresponds to Slot 1 for five samples.
 - b. Write 00000001 10000110 to the FIFO Register. This corresponds to Slot 4 for seven samples.
 - c. Write 00000001 00000100 to the FIFO Register. This corresponds to Slot 3 for five samples.

Make sure to toggle SLOT0SEL* or reselect the FIFO Register from scratch between steps 6a, 6b, and 6c.

7. Follow the procedure given in the *4. Acquisition Enable, Triggering, and Servicing* section earlier in this chapter.

Example 3

You want to scan five channels on an SCXI-1120 in Slot 4 of Chassis 1, then seven channels of an SCXI-1120 in Slot 11 of Chassis 2, three channels of an SCXI-1120 in Slot 3 in Chassis 3, and one channel of an SCXI-1120 in Slot 8 of Chassis 3.

Assuming that the modules are correctly cabled and programmed, the Slot 0 scan lists should be as follows:

Chassis 1			Chassis 2			Chassis 3		
Entry	Slot Number	Count	Entry	Slot Number	Count	Entry	Slot Number	Count
1 2	4 13	5 11	1 2 3	13 11 13	5 7 4	1 2 3	13 3 8	12 3 1

Other solutions are possible.

In the section earlier in this chapter, 3. Programming the Slot 0 Hardscan Circuitry, step 3, Write the Slot 0 scan list to the FIFO, consists of the following steps:

- 1. Select Slot 14 in Chassis 1.
- 2. Write XXXXX001 10000100 over MOSI.
- 3. Toggle SLOT0SEL*.
- 4. Write XXXX110 00001010 over MOSI.
- 5. Select Slot 14 in Chassis 2.
- 6. Write XXXX110 00000100 over MOSI.
- 7. Toggle SLOT0SEL*.
- 8. Write XXXX101 00000110 over MOSI.
- 9. Toggle SLOT0SEL*.
- 10. Write XXXX110 00000011 over MOSI.
- 11. Select Slot 14 in Chassis 3.
- 12. Write XXXX110 00001011 over MOSI.

- 13. Toggle SLOT0SEL*.
- 14. Write XXXXX001 00000010 over MOSI.
- 15. Toggle SLOT0SEL*.
- 16. Write XXXXX011 10000000 over MOSI.
- 17. Select Slot 0 in Chassis 0.

Appendix A Specifications

This appendix lists the specifications for the SCXI-1120. These are typical at 25° C unless otherwise stated. The operating temperature range is 0° to 50° C.

Analog Input

Gain (jumper-selectable)	1, 2, 5, 10, 20, 50, 100, 200, 500, 1,000, 2,000
Output range	±5 V
Number of channels	8
Gain accuracy	0.15% of full scale
Offset voltage Input Output	±6 μV ±3 mV
Stability versus ambient temperature Input offset drift Output offset drift Gain drift	±0.2 μV/°C ±200 μV/°C 20 ppm/°C
Input bias current	±80 pA
Input resistance Normal Power off Overload	40 ΜΩ 50 kΩ 50 kΩ
Output resistance Multiplexed-Output mode Parallel-Output mode	100 Ω 330 Ω
Filtering (jumper selectable)	4 Hz (-10 dB) or 10 kHz (-3 dB), 3-pole RC
Output selection time (with 5 V step, all gains) 0.012% accuracy ¹ 0.006% accuracy ² 0.0015% accuracy ²	5.2 μsec typical, 7 μsec maximum 10 μsec 20 μsec

¹Includes the combined effects of the SCXI-1120 and the AT-MIO-16F-5

²Includes the combined effects of the SCXI-1120 and the AT-MIO-16X

0.12 sec 70 μsec
0.15 V/µsec
100 nVrms 4 μVrms 150 μVrms 1 mVrms
50 or 60 Hz 250 Vrms ⁵
160 dB minimum at 4 Hz bandwidth 60 dB at 4 Hz bandwidth
250 Vrms maximum
Continuous short-to-ground
7.5 W maximum

Cold-Junction Sensor³

SCXI-1320	
Accuracy	1.0° from 0° to 55° C
Output	10 mV/°C
SCXI-1328	
Accuracy ⁴	0.35° from 15° to 35° C
2	0.65° from 0° to 15° and 35° to 55° C
Output	1.91 to 0.58 V from 0° to 55° C

¹Includes the combined effects of the SCXI-1120 and the AT-MIO-16F-5

³Located on the SCXI-1320 and SCXI-1328 terminal blocks

⁴Includes the combined effects of the temperature sensor accuracy and the temperature difference between the temperature sensor and any screw terminal

⁵Module tested using the UL 1244 standard to twice the working voltage + 1,000 Vrms

²Includes the combined effects of the SCXI-1120 and the AT-MIO-16X

You can find the temperature T (°C) as follows: Note:

 $T(^{\circ}C) = T_{K} - 273.15$

where T_K is the temperature in kelvin

$$T_{K} = \frac{1}{\left[a + b(\ln R_{T}) + c(\ln R_{T})^{3}\right]}$$

a = 1.288 x 10⁻³
b = 2.356 x 10⁻⁴
c = 9.556 x 10⁻⁸
R_{T} = resistance of the thermistor in Ω

$$R_{T} = 50,000 \left(\frac{V_{TEMPOUT}}{2.5 - V_{TEMPOUT}} \right)$$

 V_{TEMPOUT} = output voltage of the temperature sensor

Physical

Dimensions

Co

1.2 by 6.8 by 8.0 in.

nnectors	50-pin male ribbon-cable rear connector
	32-pin DIN C male front connector
	(18-screw terminal adapter available)

Operating Environment

Temperature	0° to 50° C
Relative humidity	5% to 90% at 35° C

Storage Environment

Temperature	-55° to 150° C -55° to 125° C for the SCXI-1328
Relative humidity	5% to 90% noncondensing

Appendix B Rear Signal Connector

This appendix describes the pinout and signal names for the SCXI-1120 50-pin rear signal connector, including a description of each connection.

Figure B-1 shows the pin assignments for the SCXI-1120 rear signal connector.



Figure B-1. SCXI-1120 Rear Signal Connector Pin Assignment

Rear Signal Connector Signal Descriptions

Pin	Signal Name	Description
1-2	AOGND	Analog Output Ground – Connected to the analog reference when jumper W46 is in position AB-R0.
3-18	MCH0± through MCH7±	Analog Output Channels 0 through 7 – Connects to the data acquisition board differential analog inputchannels.
19	OUTREF	Output Reference – Serves as the reference node for the analog output channels and the temperature sensor–in the DTS mode–in the Pseudodifferential Reference mode. It should be connected to the analog input sense of the NRSE data acquisition board.
24, 33	DIG GND	Digital Ground – Supply the reference for data acquisition board digital signals and are tied to the module digital ground.
25	SERDATIN	Serial Data In – Taps into the SCXIbus MOSI line to provide serial input data to a module or Slot 0.
26	SERDATOUT	Serial Data Out – Taps into the SCXIbus MISO line to accept serial output data from a module.
27	DAQD*/A	Data Acquisition Board Data/Address Line – Taps into the SCXIbus D*/A line to indicate to the module whether the incoming serial stream is data or address information.
29	SLOT0SEL*	Slot 0 Select – Taps into the SCXIbus INTR* line to indicate whether the information on MOSI is being sent to a module or Slot 0.
36	SCANCLK	Scan Clock – Indicates to the SCXI-1120 that a sample has been taken by the data acquisition board and causes the SCXI-1120 to change channels.
37	SERCLK	Serial Clock – This signal taps into the SCXIbus SPICLK line to clock the data on the MOSI and MISO lines.
43	RSVD	Reserved.

All other pins are not connected.

See the *Timing Requirements and Communication Protocol* section in Chapter 2, *Configuration and Installation*, for more detailed information on timing. Detailed signal specifications are also included in Chapter 2.

Appendix C SCXIbus Connector

This appendix describes the pinout and signal names for the SCXI-1120 96-pin SCXIbus connector, including a description of each connection.

Figure C-1 shows the pinout of the SCXI-1120 SCXIbus connector.

GUARD	Δ1	D1	GUARD
		$\varphi \circ \frac{D1}{C1}$	
GUARD			GUARD
GUARD	$A2$ \circ \circ	\circ \circ D^2	GUARD
AB0+	B2	C2	AB0-
GUARD	A3	D = D3	GUARD
GUARD	B3 V	C3	GUARD
GUARD	A4	D4	GUARD
	B4 0 0	C4	
GUARD	A5	D5	GUARD
CUARD	$\frac{AJ}{D5}$ 0 0	$\varphi \circ \frac{D5}{C5}$	CUARD
GUARD	DJ		GUARD
GUARD		o o <u>D6</u>	GUARD
	B6	C6	
	A7 0	0 0 D7	
	B7 J	C7	
	A8	D8	
	B8 0 0	0 $\frac{1}{C8}$	
	Δ <u>9</u>		
		$q \circ \frac{Dy}{C0}$	
	D9	<u> </u>	
		0 0 D10	
	B10	C10	
	A11 0 0	0 0 D11	
	B11 V	C11	
	A12	D12	
	B12 0 0	\circ \circ $C12$	
	A12	D12	
		\circ \circ $\frac{D13}{C12}$	CUICOUD
	B13	C13	CHSGND
		0 0 D14	
	B14	C14	CHSGND
	A15	D15	
	B15 Y	C15	CHSGND
	A16	D16	
	B16 0	\circ \circ $C16$	CHSGND
	A17	D17	CIISOND
	$\frac{A17}{D17}$ O Q	$\varphi \circ \frac{D17}{017}$	CURCND
	B1/	<u> </u>	CHSGND
	A18 0 0	0 0 D18	
	B18	C18	RSVD
RESET*	A19	D19	INTR*
MISO	<u>B19</u>	<u>C1</u> 9	D*/A
V-	A20	D20	V-
V-	B20 0 0	C20	V-
CHSGND	A21	D21	CHSGND
CHSGND	B21 9	\circ \circ $\frac{D21}{C21}$	CHSGND
	Δ22		V I
	<u>A22</u> 0 Q	$\varphi \circ \frac{D22}{C22}$	<u>v+</u>
<u>v+</u>	B22		<u>V+</u>
+5 V	A23 0 0	o o <u>D23</u>	+5 V
SPICLK	B23	C23	MOSI
TRIG0	A24	$D = D^{24}$	
SS*	B24 1	C24	SCANCON
	i		

Figure C-1. SCXIbus Connector Pin Assignment

SCXIbus Connector Signal Descriptions

Pin	Signal Name	Description
A1, B1, C1, D1, A2, D2, A3, B3, C3, D3, A4, D4, A5, B5, C5, D5, A6, D6	GUARD	Guard – Shields and guards the analog bus lines from noise.
B2	AB0+	Analog Bus 0+ – Positive analog bus 0 line. Used to multiplex several modules to one analog signal.
C2	AB0-	Analog Bus 0- – Negative analog bus 0 line. Used to multiplex several modules to one analog signal.
C13-C17, A21, B21, C21, D21	CHSGND	Chassis Ground – Digital and analog ground reference.
C18	RSVD	Reserved.
A19	RESET*	Reset – When pulled low, reinitializes the module to its power-up state. Totem pole. Input.
B19	MISO	Master-In-Slave-Out – Transmits data from the module to the SCXIbus. Open collector. I/O.
C19	D*/A	Data/Address – Indicates to the module whether address information or data information is being sent to the module on MOSI. Open collector. I/O.
D19	INTR*	Interrupt – Active low. Causes data that is on MOSI to be written to the Slot-Select Register Slot 0. Open collector. Output.
A20, B20, C20, D20	V-	Negative Analog Supply – -18.5 V to -25 V.
A22, B22, C22, D22	V+	Positive Analog Supply – +18.5 V to +25 V.
A23, D23	+5 V	+5 VDC Source – Digital power supply.
B23	SPICLK	Serial Peripheral Interface (SPI) Clock – Clocks the serial data on the MOSI and MISO lines. Open collector. I/O.
C23	MOSI	Master-Out-Slave-In – Transmits data from the SCXIbus to the module. Open collector. I/O.

Pin	Signal Name	Description (continued)
A24	TRIG0	TRIG0 – General-purpose trigger line used by the SCXI-1120 to send SCANCLK to other modules or receive SCANCLK from other modules. Open collector. I/O.
B24	SS*	Slot Select – When low, enables module communications over the SCXIbus. Totem pole. Input.
C24	SCANCON	Scanning Control – Combination output enable and reload signal for scanning operations. Totem pole. Input.

All other pins are not connected.

Further information is given in Chapter 3, *Theory of Operation*.

Appendix D SCXI-1120 Front Connector

This appendix describes the pinout and signal names for the SCXI-1120 front connector, including a description of each connection.

Figure D-1 shows the pin assignments for the SCXI-1120 front connector.

Pin Number	Signal Name	A Co	B C	Signal Name
22	CHO			CH0
32	C110+	T°.	•	. C110-
31	CU1	°	°	CUI
30	CHI+	\uparrow	•	CHI-
29		°	°	
28		°	°	
27	CU2	0	0	CU2
26	CH2+			-Сп2-
25	CU2	0	0	CH3
24	Спэ+		•	СПЭ-
23		°	°	
22		°	0	
21	CUA	0	0	CUA
20	Сп4+			- Сп4-
19	CI15	0	0	0115
18	CH5+	T°.	•	• СН5-
17		0	0	
16		0	0	
15	CUA	0	0	CUG
14	Сно+		•	-Спо-
13	CU7	0	0	CU7
12	СП/+			-Сп/-
11		0	0	
10		0	0	
9			0	DEVD
8				KSVD
 6	DSVD			DSVD
5	KSVD	T°.		- KS VD
3	+5 V			MTEMP
4	±3 V			- 141 1 1/1911
2 2	CHSGND			DTEMP
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Figure D-1. SCXI-1120 Front Connector Pin Assignment

Front Connector Signal Descriptions

Pin	Signal Name	Description
A2	CHSGND	Chassis Ground – Tied to the SCXI chassis.
C2	DTEMP	Direct Temperature Sensor – Connects the temperature sensor to pin 18 of the rear signal connector MCH7- when the terminal block is configured for direct temperature connection and jumper W41 is in position 3.
A4	+5 V	+5 VDC Source – Used to power the temperature sensor on the terminal block. 0.2 mA of source not protected.
C4	МТЕМР	Multiplexed Temperature Sensor – Connects the temperature sensor to the output multiplexer.
A6, C6, C8	RSVD	Reserved – Reserved for future use. Do not connect any signals to these pins. TTL/CMOS output. They are not protected.
A8, A10, C10, A16, C16,A22, C22, A28, C28	No Connect	Do not connect any signals to these pins.
A12, A14, A18, A26, A20, A24, A30, A32	CH7+ through CH0+	Positive Input Channels – The positive inputs to channels 7 through 0, respectively.
C12, C14, C18, C20, C24, C26, C30, C32	CH7- through CH0-	Negative Input Channels – The negative inputs to channels 7 through 0, respectively.

Further information is given in Chapter 2, Configuration and Installation.

Appendix E SCXI-1120 Cabling

This appendix describes how to use and install the hardware accessories for the SCXI-1120:

- SCXI-1340 cable assembly
- SCXI-1341 Lab-NB, Lab-PC, and Lab-PC+ cable assembly
- SCXI-1342 PC-LPM-16 cable assembly
- SCXI-1344 Lab-LC cable assembly
- SCXI-1180 feedthrough panel
- SCXI-1302 50-pin terminal block
- SCXI-1351 one-slot cable extender
- SCXI-1350 multichassis adapter
- SCXI-1343 screw terminal adapter

SCXI-1340 Cable Assembly

The SCXI-1340 cable assembly connects an MIO-16 board to an SCXI-1120 module. The SCXI-1340 consists of a 50-conductor ribbon cable that has mounting bracket at one end and a 50-pin female connector at the other end. The female connector connects to the I/O connector of the MIO-16 board. Attached to the mounting bracket is a 50-pin female mounting-bracket connector that connects to the module rear signal connector. To extend the signals of the MIO-16 board to an SCXI-1180 feedthrough panel or an SCXI-1181 breadboard module, you can use the male breakout connector that is near the mounting bracket on the ribbon cable. All 50 pins from the MIO-16 board go straight through to the rear signal connector. You can use a standard 50-pin ribbon cable instead of the SCXI-1340 cable assembly. The SCXI-1340 has the following advantages over the ribbon cable:

- The SCXI-1340 has strain relief so that you cannot accidentally disconnect the cable.
- The SCXI-1340 includes a mounting bracket that mounts to the chassis so that you can remove and reinsert the module without explicitly removing the cable from the back of the chassis. This is especially useful when the SCXI chassis is rack mounted, making rear access difficult.
- The SCXI-1340 has an extra male breakout connector for use with the SCXI-1180 feedthrough panel or additional modules or breadboards that need a direct connection to the MIO-16 board.
- The SCXI-1340 rear panel gives the module and the chassis both mechanical and electrical shielding.

Table E-1 lists the pin equivalences of the MIO-16 board and the SCXI-1120.

Pin	SCXI-1120 Rear Signal Connector	MIO-16 Board Equivalent
1-2	AOGND	AIGND
3	MCH0+	ACH0
4	MCH0-	ACH8
5	MCH1+	ACH1
6	MCH1-	ACH9
7	MCH2+	ACH2
8	MCH2-	ACH10
9	MCH3+	ACH3
10	MCH3-	ACH11
11	MCH4+	ACH4
12	MCH4-	ACH12
13	MCH5+	ACH5
14	MCH5-	ACH13
15	MCH6+	ACH6
16	MCH6-	ACH14
17	MCH7+	ACH7
18	MCH7-	ACH15
19	OUTREF	AISENSE
24, 33	DIG GND	DIG GND
25	SERDATIN	ADIO0
26	SERDATOUT	BDIO0
27	DAQD*/A	ADIO1
29	SLOT0SEL*	ADIO2
36	SCANCLK	SCANCLK
37	SERCLK	EXTSTROBE*
43	RSVD	OUT1

Table E-1. SCXI-1120 and MIO-16 Board Pinout Equivalences

No other pins are connected on the SCXI-1120.

SCXI-1340 Installation

Follow these steps to install the SCXI-1340:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module in the chassis.
- 3. Plug the mounting bracket connector onto the module rear signal connector (see Figure E-1). Make sure the alignment tab on the bracket enters the upper module guide of the chassis.
- 4. Screw the mounting bracket to the threaded strips in the rear of the chassis.

5. Connect the loose end of the cable assembly to the MIO-16 board rear signal connector.

Check the installation.

After step 1, the order of these steps is not critical; however, it is easier to locate the correct position for the mounting bracket with a module installed in the chassis. If you will attach a cable to the breakout connector, installation is easiest if you attach the second cable before installing the SCXI-1340.



Figure E-1. SCXI-1340 Installation

SCXI-1341 Lab-NB, Lab-PC, or Lab-PC+ and SCXI-1344 Lab-LC Cable Assembly

The SCXI-1341 Lab-NB, Lab-PC, or Lab-PC+ cable assembly connects a Lab-NB, Lab-PC, or Lab-PC+ board to an SCXI-1120 module. The SCXI-1344 Lab-LC cable assembly connects a Lab-LC board to an SCXI-1120 module. The SCXI-1341 and SCXI-1344 cable assemblies consist of two pieces—an adapter board and a 50-conductor ribbon cable that connects the Lab board to the rear connector of the adapter board. The adapter board converts the signals from the Lab board I/O connector to a format compatible with the SCXI-1120 rear signal connector pinout at the front connector of the SCXI-1341 or SCXI-1344. The adapter board also has an additional male breakout connector that makes the unmodified Lab board signals accessible to an SCXI-1180 feedthrough panel or an SCXI-1181 breadboard module. The adapter board gives the

Lab boards full access to the digital control lines and analog signals (except DTEMP), but the Lab boards cannot scan channels in Multiplexed mode. Leave jumper W1 in position A on the SCXI-1341 and SCXI-1344. The SCXI-1120 does not use jumper W1. Table E-2 lists the SCXI-1341 and SCXI-1344 pin translations.

Note: If you are using the Lab-PC+, configure the board for single-ended inputs.

Lab Board Pin	Lab Board Signal	SCXI-1120 Pin	SCXI-1120 Signal
1	ACH0	3	MCH0+
2	ACH1	5	MCH1+
3	ACH2	7	MCH2+
4	ACH3	9	MCH3+
5	ACH4	11	MCH4+
6	ACH5	13	MCH5+
7	ACH6	15	MCH6+
8	ACH7	17	MCH7+
9	AIGND	1-2	AOGND
10	DAC0OUT	20	No Connect
11	AOGND	23	No Connect
12	DAC10UT	21	No Connect
13, 50	DGND	24, 33	DIG GND
26	PB4	25	SERDATIN
27	PB5	27	DAQD*/A
28	PB6	29	SLOT0SEL*
29	PB7	37	SERCLK
31	PC1	26	SERDATOUT
32	PC2	28	No Connect
40	EXTCONV*	36	SCANCLK
43	OUTB1	46	No Connect
49	+5 V	34-35	No Connect

Table E-2. SCXI-1341 and SCXI-1344 Pin Translations

All other pins of the Lab board pinout are not sent to the SCXI-1120 rear signal connector.

SCXI-1341 and SCXI-1344 Installation

Follow these steps to install the SCXI-1341 or SCXI-1344:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module in the chassis.
- 3. Connect one end of the ribbon cable to the adapter board rear connector. This is the 50-pin connector of the SCXI-1344 cable.
- 4. Plug the adapter board front connector to the module rear signal connector. Make sure a corner of the adapter board enters the upper module guide of the chassis.
- 5. Screw the rear panel to the threaded strips in the rear of the chassis.

6. For an SCXI-1341, connect the loose end of the ribbon cable to the Lab-NB, Lab-PC, or Lab-PC+ I/O connector. For an SCXI-1344, connect the two 26-pin connectors to the Lab--LC according to the instructions given in the *Installation* section of Chapter 2, *Configuration and Installation*, of the *Lab-LC User Manual*.

Check the installation.

SCXI-1342 PC-LPM-16 Cable Assembly

The SCXI-1342 PC-LPM-16 cable assembly connects a PC-LPM-16 board to an SCXI-1120 module. The 1342 cable assembly consists of two pieces—an adapter board and a 50-conductor ribbon cable that connects the PC-LPM-16 board to the adapter board. The adapter board converts the signals from the PC-LPM-16 I/O connector to a format compatible with the SCXI-1120 rear signal connector pinout. The adapter board also has an additional male breakout connector that makes the unmodified PC-LPM-16 signals accessible to an SCXI-1180 feedthrough panel or SCXI-1181 breadboard module. The adapter board gives the PC-LPM-16 full access to the digital control lines and analog signals, but the PC-LPM-16 cannot scan channels in the Multiplexed mode. Leave jumper W1 in position A on the SCXI-1342. The SCXI-1120 does not use jumper W1. Table E-3 lists the SCXI-1342 pin translations.

PC-LPM-16 Pin	PC-LPM-16 Signal	Rear Signal Connector Pin	SCXI-1120 Use
1-2	AIGND	1-2	AOGND
3	ACH0	3	MCH0+
4	ACH8	4	MCH0-
5	ACH1	5	MCH1+
6	ACH9	6	MCH1-
7	ACH2	7	MCH2+
8	ACH10	8	MCH2-
9	ACH3	9	MCH3+
10	ACH11	10	MCH3-
11	ACH4	11	MCH4+
12	ACH12	12	MCH4-
13	ACH5	13	MCH5+
14	ACH13	14	MCH5-
15	ACH6	15	MCH6+
16	ACH14	16	MCH6-
17	ACH7	17	MCH7+
18	ACH15	18	MCH7-
19, 50	DGND	24, 33	DIG GND
28	DIN6	26	SERDATOUT
29	DIN7	28	No Connect
34	DOUT4	25	SERDATIN
35	DOUT5	27	DAQD*/A

Table E-3.	SCXI-1342 Pin	Translations

(continues)

PC-LPM-16 Pin	PC-LPM-16 Signal	Rear Signal Connector Pin	SCXI-1120 Use
36	DOUT6	29	SLOT0SEL*
37	DOUT7	37	SERCLK
46	OUT2	46	No Connect
49	+5 V	34-35	No Connect

Table E-3.	SCXI-1342 Pin	Translations ((Continued)
I dole L D.	Sour is a im	I failofactorio	(commaca)

All other pins of the PC-LPM-16 pinout are not sent to the SCXI-1120 rear signal connector.

SCXI-1342 Installation

Follow these steps to install the SCXI-1342:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module to which the SCXI-1342 will connect.
- 3. Connect one end of the ribbon cable to the adapter board rear connector.
- 4. Plug the adapter board front connector onto the module rear signal connector. Make sure a corner of the adapter board enters the upper module guide of the chassis.
- 5. Screw the rear panel to the threaded strips in the rear of the chassis.
- 6. Connect the loose end of the ribbon cable to the PC-LPM-16 I/O connector.

Check the installation.

SCXI-1180 Feedthrough Panel

The SCXI-1180 feedthrough panel provides front-panel access to the signals of any data acquisition board that uses a 50-pin I/O connector. The SCXI-1180 consists of a front panel with a 50-pin male front panel connector that occupies one slot in the SCXI chassis, and a ribbon cable with a female rear connector and a male breakout connector. You can attach the rear connector to the male breakout connector of an SCXI-1340, SCXI-1341, SCXI-1342, SCXI-1344, or SCXI-1351 in the adjacent slot. The breakout connector further extends the cabling scheme. The front panel connector provides the feedthrough connection. You can attach an SCXI-1302 terminal block to the front panel connector for simple screw terminal connections. A rear filler panel that shields and protects the interior of the SCXI chassis is also included.

SCXI-1180 Installation

Install the SCXI-1180 to the right of a slot that has an SCXI-1340, SCXI-1341, SCXI-1342, or SCXI-1344 cable assembly or an SCXI-1351 slot extender in its rear connector space.

Follow these steps to install the SCXI-1180:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Remove the front filler panel of the slot where you will insert the SCXI-1180.
- 3. Thread the rear connector through the front of the chassis to the rear of the chassis. Attach the rear connector to the breakout connector of the adjacent cable assembly or slot extender, as shown in Figure E-2.



Figure E-2. SCXI-1180 Rear Connections

- 4. Screw in the rear panel to the threaded strip in the rear of the chassis.
- 5. Screw the front panel into the front threaded strip, as shown in Figure E-3.

Check the installation.



Figure E-3. SCXI-1180 Front Panel Installation

SCXI-1302 50-Pin Terminal Block

The SCXI-1302 terminal block has screw terminal connections for the 50-pin connector on the SCXI-1180 feedthrough panel.

SCXI-1302 Wiring Procedure

To wire the SCXI-1302 terminal block, you must remove the cover, connect all the wiring, and replace the cover. The procedure for this is as follows:

- 1. Unscrew the rear grounding screw on the back of the terminal block, as shown in Figure E-4.
- 2. With a flathead screwdriver, carefully pry the cover off the terminal block.
- 3. Insert each wire through the terminal block strain-relief opening.
- 4. Connect the wires to the screw terminals.
- 5. Tighten the large strain-relief screws to secure the wires.
- 6. Snap the cover back in place.
- 7. Reinsert the rear grounding screw. The terminal block is now ready to be connected to the front panel connector.



Figure E-4. Cover Removal

SCXI-1302 Installation

Follow these steps to install the SCXI-1302:

- 1. Install an SCXI-1180 feedthrough panel as described in the SCXI-1180 Installation section.
- 2. Wire the terminal block as previously described in the SCXI-1302 Wiring Procedure section.
- 3. Connect the SCXI-1302 terminal block to the front panel connector on the SCXI-1180 feedthrough panel. Be careful to fit the thumbscrews in the thumbscrew cutouts.
- 4. Tighten the top and bottom captive screws on the back of the terminal block into the screw holes in the front panel. This will hold the SCXI-1302 securely in place.

Check the installation.

SCXI-1351 One-Slot Cable Extender

The SCXI-1351 cable extender is a miniature SCXI-1340 cable assembly. Instead of connecting to an MIO board 1 m away, the SCXI-1351 female rear connector connects to the male breakout connector of a module that must be in the rear connector space of the slot to the left. The SCXI-1351 has a female mounting bracket connector that mates with the rear signal connector of a module, and also has a male breakout connector on the ribbon cable for connecting to a feedthrough panel or more cable extenders.

SCXI-1351 Installation

Follow these steps to install the SCXI-1351:

- 1. Make sure that the computer and the SCXI chassis are turned off.
- 2. Install the SCXI module in the chassis.
- 3. Connect the rear connector of the cable extender to the breakout connector in the adjacent slot. This attachment is similar to Step 3 in the *SCXI-1180 Installation* section, as shown in Figure E-2.
- 4. Plug the mounting bracket connector to the module rear signal connector. Make sure the alignment tab on the bracket enters the upper module guide of the chassis.
- 5. Screw the mounting bracket to the threaded strips in the rear of the chassis.

Check the installation.

SCXI-1350 Multichassis Adapter

You use the SCXI-1350 multichassis adapter to connect an additional SCXI-1001 chassis to the MIO-16 board. Using several SCXI-1350s, you can connect up to eight chassis to a single MIO board. The SCXI-1350 consists of a multichassis adapter board. You will also need a ribbon cable for each chassis-to-chassis connection, and a ribbon cable for the connection from the MIO board to the first chassis.

Note: Use 0.5 m ribbon cable when connecting multiple chassis together to minimize cable length and maintain signal integrity. You can use a 1 m cable from the MIO board to the first chassis.

The adapter board has a male rear connector, a female front connector, and a male chassis extender connector. You can attach the rear connector to a ribbon cable from the MIO board or a preceding chassis. You connect the front connector with the module rear signal connector. You connect the chassis extender connector to a ribbon cable that goes to the subsequent chassis. The adapter takes Channel 0 from the front connector and sends it to Channel 0 of the rear connector. The adapter also takes channels 0 through 6 on the chassis extender connector and maps them to channels 1 through 7, respectively, on the rear connector.

SCXI-1350 Installation

Follow these steps to install the SCXI-1350:

- 1. Make sure that the computer and all the SCXI chassis are turned off.
- 2. Insert all the modules in all the chassis.
- 3. Connect one end of a ribbon cable to the MIO board.
- 4. Connect the other end of the ribbon cable to the rear connector of the first SCXI-1350.
- 5. Connect another ribbon cable or cable assembly to the chassis extender connector.
- 6. Plug the adapter board front connector to the module rear signal connector. Make sure a corner of the adapter board enters the upper module guide of the chassis.
- 7. Screw the rear panel to the threaded strips in the rear of the chassis.
- 8. Connect the cable assembly to the desired module in the second chassis, or if you are using more than two chassis, connect the loose end of the ribbon cable to the rear connector of the second SCXI-1350, and install the adapter board.
- 9. Continue until all chassis are connected. For *N* chassis, you will need *N* ribbon cables and *N* multichassis adapters.

SCXI-1343 Rear Screw Terminal Adapter

You use the SCXI-1343 universal adapter to adapt custom wiring to the SCXI-1120. The SCXI-1343 has screw terminals for the analog output connections and solder pads for the rest of the signals. A strain-relief clamp is on the outside of the rear panel.

SCXI-1343 Installation

- 1. Insert each wire through the adapter strain-relief opening.
- 2. Make all solder connections first.
- 3. Connect the other wires to the screw terminals.
- 4. Tighten the strain-relief screws to secure the wires.
- 5. Plug the adapter board front connector to the module rear signal connector. Make sure a corner of the adapter board enters the upper module guide of the chassis.
- 6. Screw the rear panel to the threaded strips in the rear of the chassis.

Rear Signal Connector Pin	SCXI-1120 Use	Connection Type
1	AOGND	Solder pad
2	AOGND	Screw terminal
3	MCH0+	Screw terminal
4	MCH0-	Screw terminal
5	MCH1+	Screw terminal
6	MCH1-	Screw terminal
7	MCH2+	Screw terminal
8	MCH2-	Screw terminal
9	MCH3+	Screw terminal
10	MCH3-	Screw terminal
11	MCH4+	Screw terminal
12	MCH4-	Screw terminal
13	MCH5+	Screw terminal
14	MCH5-	Screw terminal
15	MCH6+	Screw terminal
16	MCH6-	Screw terminal
17	MCH7+	Screw terminal
18	MCH7-	Screw terminal
19	OUTREF	Screw terminal
20	No Connect	Solder pad
21	No Connect	Solder pad
22	No Connect	Solder pad
23	No Connect	Solder pad
24, 33	DIG GND	Solder pad
26	SERDATOUT	Solder pad
27	DAQD*/A	Solder pad
28	No Connect	Solder pad
29	SLOT0SEL*	Solder pad
30	No Connect	Solder pad
31	No Connect	Solder pad
32	No Connect	Solder pad
33	No Connect	Solder pad
34-35	No Connect	Solder pad
36	SCANCLK	Solder pad
37	SERCLK	Solder pad
38	No Connect	Solder pad
39	No Connect	Solder pad
40	No Connect	Solder pad
41	No Connect	Solder pad
42	No Connect	Solder pad
43	RSVD	Solder pad
44	No Connect	Solder pad
45	No Connect	Solder pad
46	No Connect	Solder pad
47	No Connect	Solder pad
48	No Connect	Solder pad
49	No Connect	Solder pad
50	No Connect	Solder pad

Appendix F Revision A and B Photo and Parts Locator Diagrams

This appendix contains a photograph of the Revision A and B SCXI-1120 signal conditioning module and the general and detailed parts locator diagrams.

Figure F-1 shows the Revision A and B SCXI-1120 signal conditioning module. Figures F-2 and F-3 show the general and detailed parts locator diagrams.







Appendix G Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve technical problems you might have as well as a form you can use to comment on the product documentation. Filling out a copy of the *Technical Support Form* before contacting National Instruments helps us help you better and faster.

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)
Processor
MB Display adapter
adapters installed
Revision
Version

SCXI-1120 Hardware Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

- SCXI-1120 Revision Letter
- Chassis Slot
- Chassis Type
- Grounding, Shielding, and Reference Mode Selection (Factory Setting: Parked, W46, B-R0R1)
- Input Channel Gain Configuration

Input Channel	First-Stag	ge Gain	Second-Sta	age Gain	Total Gain
	Factory Setting	User Setting	Factory Setting	User Setting	Factory Setting, 1,000
0	100, W1, A		10, W9, D		
1	100, W2, A		10, W10, D		
2	100, W3, A		10, W11, D		
3	100, W4, A		10, W12, D		
4	100, W5, A		10, W13, D		
5	100, W6, A		10, W14, D		
6	100, W7, A		10, W15, D		
7	100, W8, A		10, W16, D		

• Input Channel Filter Configuration

Input Channel	Factory Setting	User Setting
0	W17, A, W25, ON, W26, OFF	
1	W18, A, W27, ON, W28, OFF	
2	W19, A, W29, ON, W30, OFF	
3	W20, A, W31, ON, W32, OFF	
4	W21, A, W33, ON, W34, OFF	
5	W22, A, W35, ON, W36, OFF	
6	W23, A, W37, ON, W38, OFF	
7	W24, A, W39, ON, W40, OFF	

- Other Modules in System
- Data Acquisition Boards Installed

Documentation Comment Form

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SCXI-1120 User Manual

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Glossary

Prefix	Meaning	Value
p- n- μ- m- k- Μ-	pico- nano- micro- milli- kilo- mega-	$ \begin{array}{r} 10^{-12} \\ 10^{-9} \\ 10^{-6} \\ 10^{-3} \\ 10^{3} \\ 10^{6} \\ \end{array} $

Numbers/Symbols

0	degrees
Ω	ohms
+5 V (signal)	+5 VDC Source signal

Α

А	amperes
AB0+	Positive Analog Bus 0 signal
AB0-	Negative Analog Bus 0 signal
AB0EN	Analog Bus 0 Enable bit
ACH#	data acquisition board Analog Input Channel Number
A/D	analog-to-digital
AOGND	Analog Output Ground signal
Arms	amperes, root mean square
AWG	American Wire Gauge
Ð	
В	
BW	bandwidth
С	
С	Celsius
CH#+	Positive Input Channel Number signal
CH#-	Negative Input Channel Number signal
CHAN	Channel Select bit
CHS	Chassis bit
CHSGND	Chassis Ground signal
CJR	cold-junction reference
CLKEN	Clock Enable bit

Scan Clock Output Enable bit

Scan Clock Select bit

Count bit

CLKOUTEN CLKSELECT

CNT

D

DTEMP Direct Temperature Sensor signal	D*/A D/A DAQD*/A dB DIG GND DIN DMM	Data/Address signal digital-to-analog Data Acquisition Board Data/Address Line signal decibels Digital Ground signal Deutsche Industrie Norme digital multimeter
DTC direct temperature concer	DIN DMM DTEMP DTS	Deutsche Industrie Norme digital multimeter Direct Temperature Sensor signal

F

F	Fahrenheit
FIFO	first-in-first-out
FOUTEN*	Forced Output Enable bit
FRT	Forced Retransmit bit

G

GBWP	gain bandwidth product
GUARD	Guard signal

Η

hex	hexadecimal
HSCR	Hardscan Control Register
HSRS*	Hardscan Reset bit
Hz	hertz

I

II	input current leakage
in.	inches
INTR*	Interrupt signal
I/O	input/output

K

K	kelvin
K	Kelvin

L

LOAD*	Load bit
LSB	least significant bit

Μ

m M MCH#+ MCH#- MIO MISO MOD MOSI MSB MTEMP MTS	meters megabytes of memory Positive Analog Output Channel Number signal Negative Analog Output Channel Number signal multifunction I/O Master-In-Slave-Out signal Module Number bit Master-Out-Slave-In signal most significant bit Multiplexed Temperature Sensor signal multiplexed temperature sensor
Ν	
NRSE	nonreferenced single-ended (input)
0	
ONCE OUTREF	Once bit Output Reference signal
Р	
ppm	parts per million
R	
RAM RD RESET* rms RSE RSVD RTD RTEMP RTSI	random-access memory Read bit Reset signal root mean square referenced single-ended (input) Reserved bit/signal resistance temperature detector Read Temperature bit Real-Time System Integration
S	
SCANCLK SCANCLKEN SCANCON SCANCONEN SCXI SDK	Scan Clock signal Scan Clock Enable bit Scanning Control signal Scan Control Enable bit Signal Conditioning eXtensions for Instrumentation (bus) Software Developer's Kit

Glossary

sec SERCLK SERDATIN SERDATOUT SL SLOT0SEL* SPI SPICLK SS*	seconds Serial Clock signal Serial Data In signal Serial Data Out signal Slot bit Slot 0 Select signal Serial Peripheral Interface Serial Peripheral Interface Clock signal Slot Select signal
Т	
tempco TRIG0	temperature coefficient Trigger 0 signal
U	
UL	Underwriters Laboratory
V	
$V \\ V+ \\ V- \\ VDC \\ V_{IH} \\ V_{IL} \\ V_{OH} \\ V_{OL} \\ Vrms$	volts Positive Analog Supply signal Negative Analog Supply signal volts direct current input logic high voltage input logic low voltage output logic high voltage output logic low voltage volts, root mean square
W	
W	watts

Numbers/Symbols

+5 V signal front connector, 2-13, D-2 SCXIbus connector, 3-4, C-3

A

AB0- signal, 3-4, C-3 AB0+ signal, 3-4, C-3 AB0EN bit, 4-4 AC-coupled signal connection with high common-mode voltage, 2-15 analog configuration direct temperature connection (jumper W41), 2-8 to 2-9 filter jumpers, 2-10 gain jumpers, 2-9 to 2-10 grounding, shielding, and referencemode selection (jumper W46), 2-7analog input channels analog input block diagram, 3-9 calibration, 3-10 to 3-12 equipment requirements, 3-10 to 3-11 offset null adjust, 3-11 potentiometers reference designators, 3-12 formula for determining overall gain, 3-10 front connector, 2-12 to 2-13 AC-coupled signal connection, 2-15 floating AC-coupled signal connection, 2-14 floating signal connection, 2-14 ground-referenced signal connection, 2-14 warning against exceeding input range, 2-15 theory of operation, 3-8 to 3-10 analog input specifications, A-1 to A-2 analog output circuitry, 3-12 to 3-13 analog output signal connections, 2-26

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